Neutrons atmosphériques en avionique

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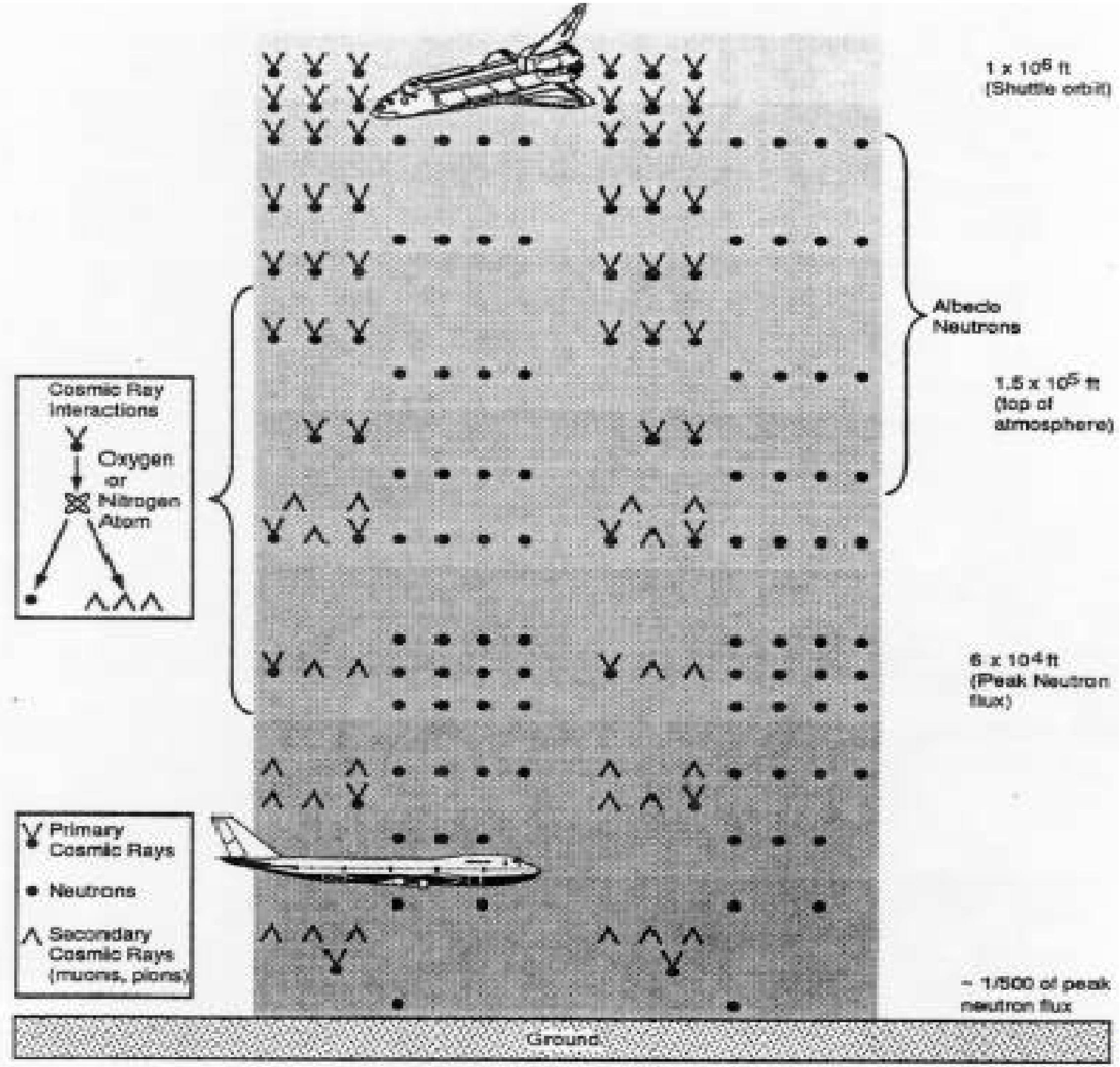
Sommaire

Radiation Environment

Three primary radiation components of the natural space environment affect CMOS devices :

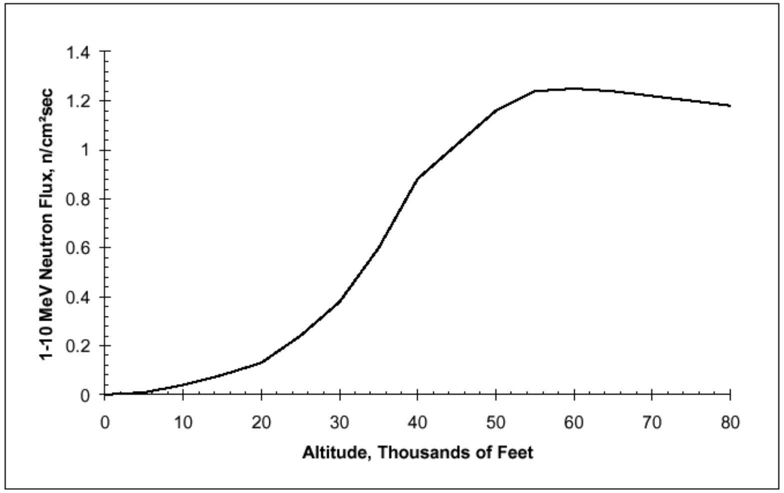
- First, planetary magnetic fields trap belts of high-energy Protons and electrons, thus subjecting satellites to large fluxes of these particles when they pass through the radiation belts.
- Second, galactic cosmic rays occur everywhere in space. These highly energetic particles, with a wide range of atomic numbers, exist in a very low flux compared to the number of particles in the radiation belts. However, a single galactic cosmic ray can deposit sufficient charge in a modern integrated circuit to change the state of internal storage elements and may also cause more complex internal behavior.
- Third, solar flares produce varying quantities of electrons, Protons, and lower energy charged particles. Solar flare activity varies widely at different times. During periods of high solar activity, very high fluxes of particles may occur over time periods of hours or days.

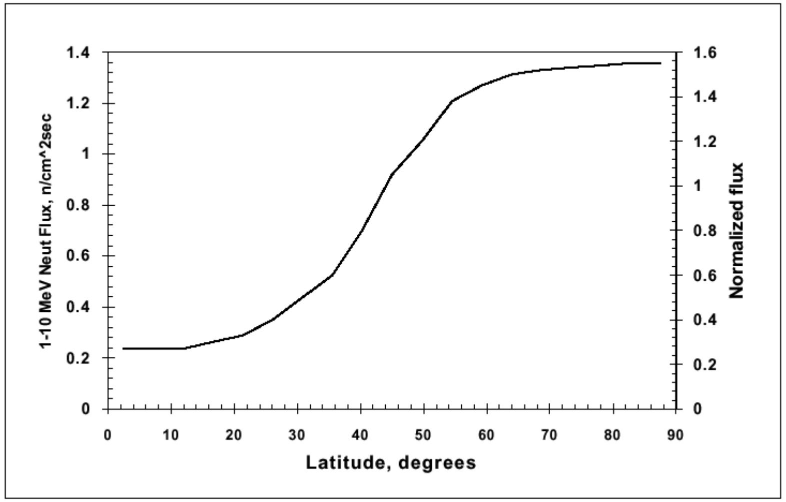
Neutron Environment in the Atmosphere



- Neutrons are created by cosmic ray interactions with the O_2 and N_2 in the air.
  - peak at ~60,000 ft, the peak flux is ~4 Neutron/cm_/sec.
  - At 30,000 ft the Neutrons are about 1/3 the peak flux.
  - On the ground, ~1/400 of the peak flux.
- Other particles such as secondary Protons and pions are also created,
  but for SEU the Neutrons are the most important.

Effects of altitude and latitude



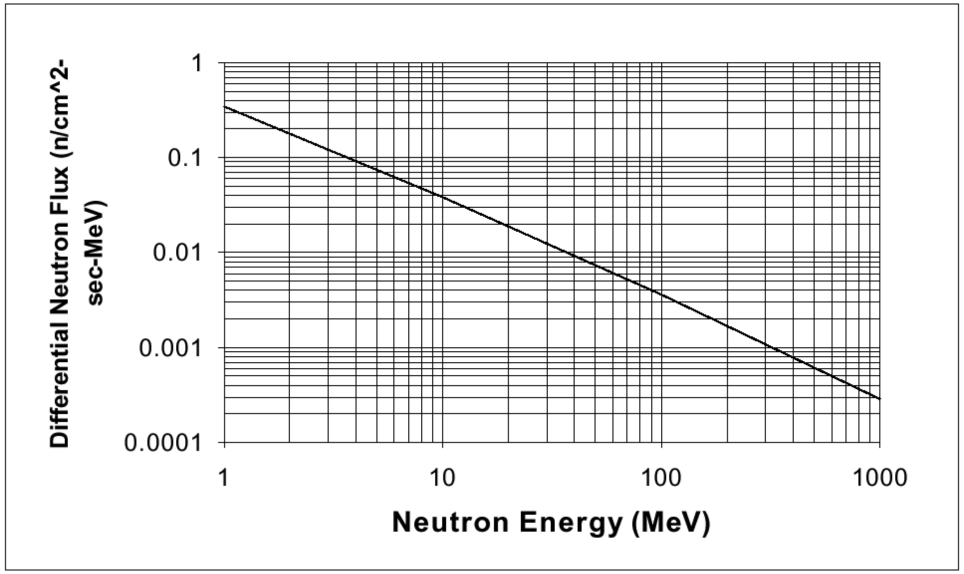


The Neutrons in the atmosphere vary with both altitude and latitude as shown by the figures beside.

The altitude variation derives from the competition between the various production and removal processes that affect how the Neutrons and the initiating cosmic rays interact with the atmosphere.

The latitude variation of the 1-10 MeV atmospheric Neutron is based on measurements made aboard aircraft at 35,000 feet.

Neutron Energy



The Neutrons extend in energy to up to 1000 MeV.

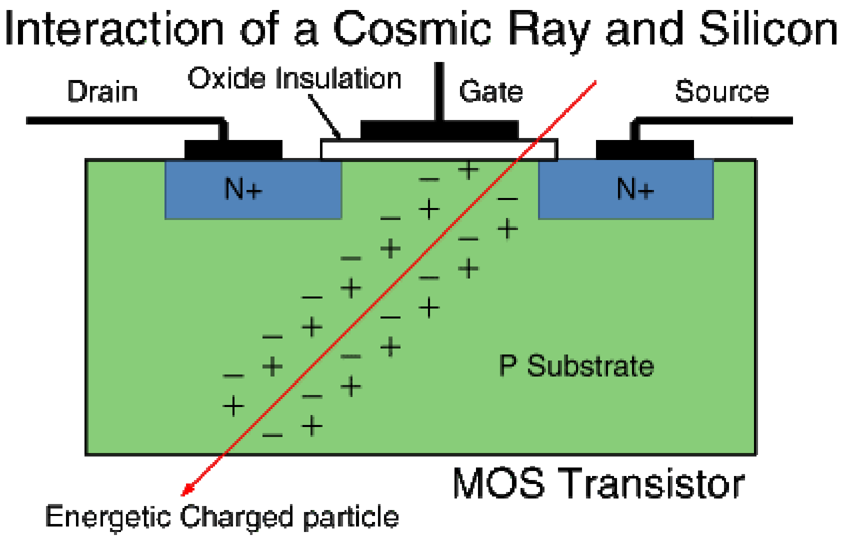
The figure beside shows the differential Neutron energy spectrum as measured by Hewitt et al.

It applies at 40,000 feet and 45° latitude.

Neutron Single Event Effect (SEE)

- Atmospheric Neutrons have been identified as the main cause of single event effects (SEE) at elevated altitudes
- Neutrons cause single event upset (SEU) not through direct ionization, but rather through nuclear reactions with the silicon resulting in recoils that can deposit enough energy in the sensitive volume to generate an upset.
- Other effects :
  - SEL : Single Event Latch-up
  - SEB : Single Event Burn-out (power device)
  - SET : Single Event Transient (analog circuit)

Interaction of a Cosmic Ray with Silicon



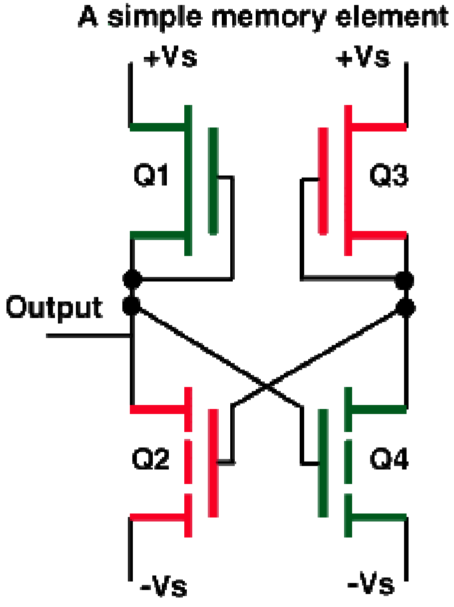
A particle passing through matter (for example, silicon) transfers its energy to the medium primarily by ionizing atoms along its path. The particle produces charges along its path, in the form of electrons and holes. These are collected at the source and drain, and a current pulse appears. This can be large enough to produce an effect like that of a normal signal applied to the transistor.

SEU (Single-Event Upset) Definition

A high-energy ion induces a short-duration pulse of current in a p-n junction, such as the drain region.
If the charge collected at the drain of a CMOS storage element (e.g., memory or flip-flop) exceeds the **critical charge** required to switch the circuit, it will change state, and the information that was previously stored will be lost. Even though the circuit changes state, it still functions normally, and reinitializing or rewriting can **restore** its original configuration.

Originally, only **heavy ions** caused SEU effects.
As individual transistors were scaled to smaller dimensions to increase the size and complexity of VLSI circuits, their susceptibility to SEU effects has increased sufficiently to be upset with **Protons and Neutrons** (through nuclear reactions) as well as with heavy particles.

How an SEU (bit-flip) Occurs



The image beside shows a simple 1-bit storage device illustrating the effect of an SEU, or "bit-flip." The circuit is designed so that it has two stable states, one that represents a stored '0' and one that represents a stored '1.' In each state, two transistors are turned on and two are turned off.

A bit-flip occurs when an energetic particle causes the state of the transistors in the circuit to reverse. This phenomenon occurs in many microcircuits, including memory chips and microprocessors.

MBU (Multiple-Bit Upset) Definition

- For some technologies, such as DRAMs, SDRAMs or SRAMs, the ionization track from a single particle may cause several storage elements in a circuit to upset. This is called "multiple-bit upset”. This phenomenon is more difficult to deal with than SEU because the multiple errors may interfere with system-level approaches such as **error-detection-and-correction** (EDAC) that are often used to overcome SEU effects.
  It has to be noticed that this effect depends of the **geographical implantation** of the die.
- A second type of MBU can be considered when a particle affects not a storage element but a control element of a part resulting in a wrong behavior, lockup, hard error, etc.. This is called Functional MBU or **Functional interrupt (SEFI).**
- As a result of a SAAB study (concerning SRAM), the ratio between MBU and SEU is about **0,5%.**

Basic definition : CROSS SECTION

- For a fixed particle energy, we designate the sensitivity of the circuit with **P_{err} = *Prob* (error / particle hit)**.

  This sensitivity is less than one because not all parts of a chip are sensitive to particles (e.g., empty areas or areas with only wires and no transistors underneath).

  If the chip area is A_{chip} , the total sensitive area of the chip will be

  $\sigma = P_{err} \times A_{chip}$ (Unit = cm^2)

  σ is known as the ***cross section*** of the device.

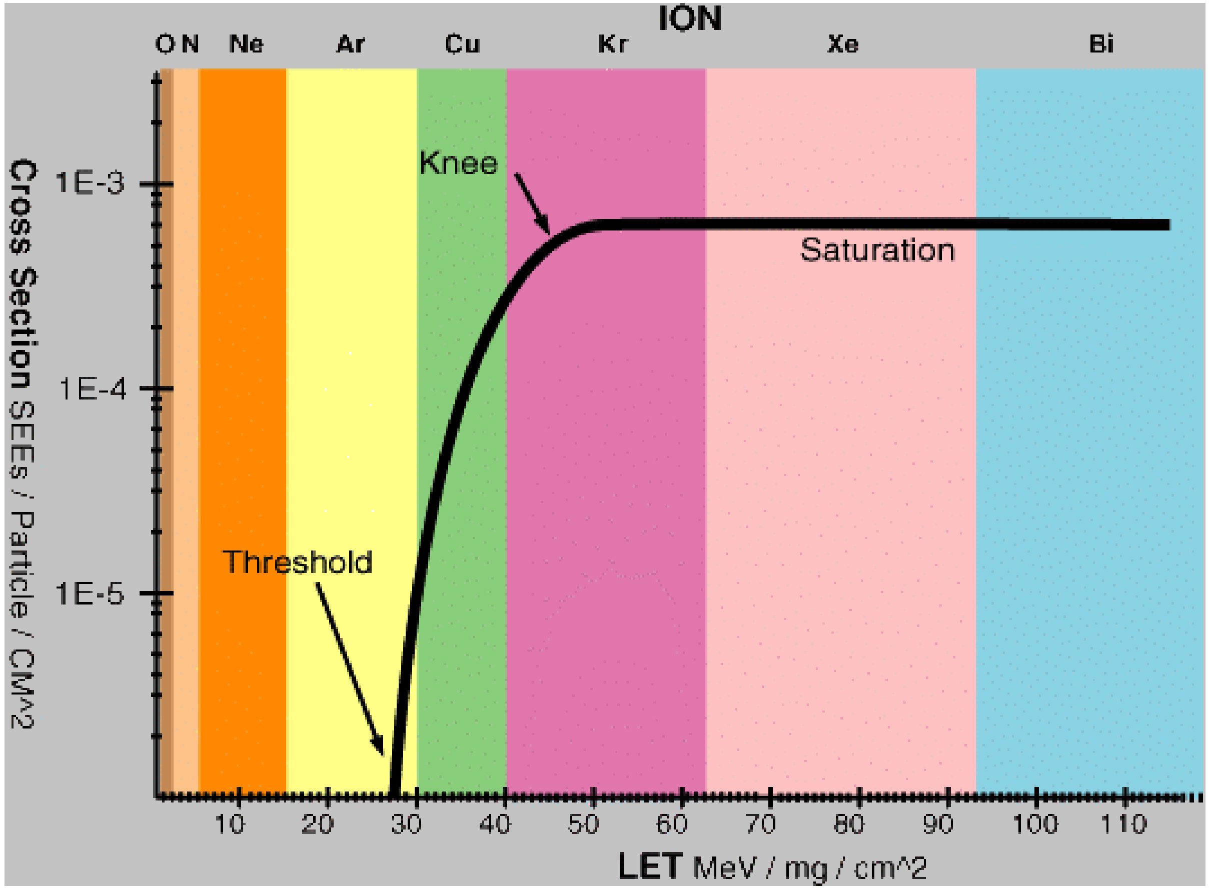
- The cross section per bit is also often used.
  If N is the number of bit of the circuit, the cross section per bit is :

  $\sigma_{bit} = \sigma / N$ (Unit = cm^2/bit)

Basic definition : LET

- A particle's ionization loss-rate is called **Linear Energy Transfer** (LET)
- The amount of energy deposited (and therefore, charge created) in a vulnerable region of a circuit component is proportional to LET x path length in the region. By convention, "path length" is measured in units of mass per unit area (mg / cm^2) and energy in MeV. Thus, LET has the units of **MeV x cm^2 / mg**
- With most devices, there is some minimum LET that is required to affect the part. This minimum LET is called the **threshold LET**. Above the threshold LET, there is a range where, as the LET increases, the cross-section also increases. As LET gets larger, eventually a point is reached, called the knee, where an increase in LET no longer affects upset rate. All particles with LET higher than the knee value affect the part equally.

Typical curve : Cross section / LET



Basic definition : SEU rate

- One important metric for radiation damage is the rate at which errors occur in the circuit. This rate is often referred to as ***soft error rate* (*SER*).** It is also called Upset rate or SEU rate.

  To calculate the rate at which SEUs occur in the circuit, we start with the rate at which particles hit the circuit.
  Particle hit rate, or ***flux***, is measured in (particles/cm^2)/h.

  The error rate of a circuit is : ***SEU rate = flux X*** σ

  (with **σ** = cross section of the circuit) (Unit : /h)

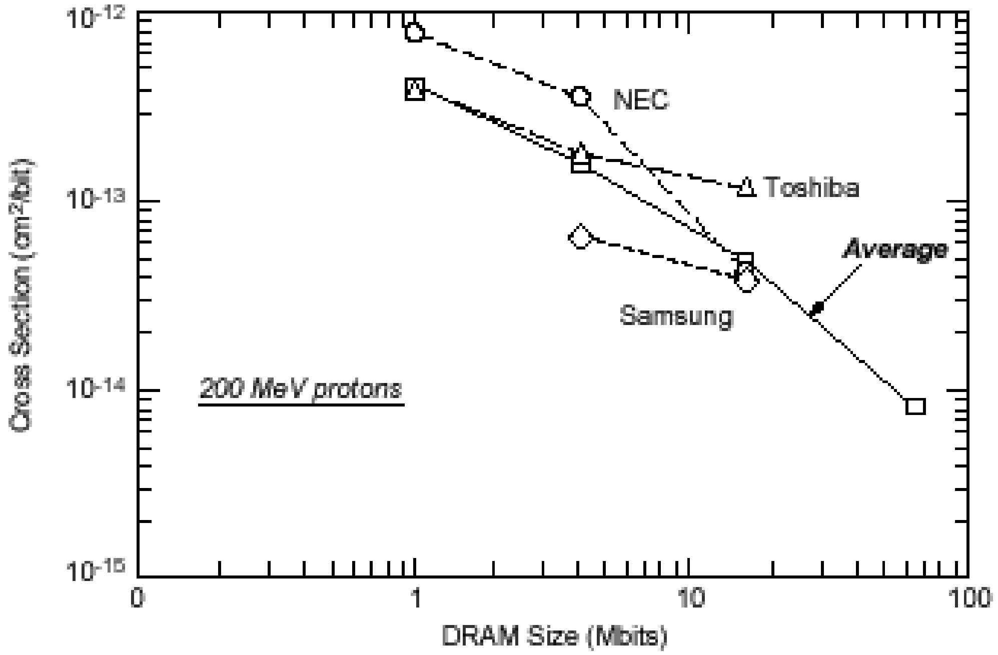
  We can also consider a SEU rate per bit which is :

$$\textit{\textbf{SEU rate}}_{/bit} = \textit{\textbf{SEU rate}}_{/circuit} \,/\, \textit{\textbf{N}}$$

  (with N = number of bit of the circuit) (Unit : /bit/h)

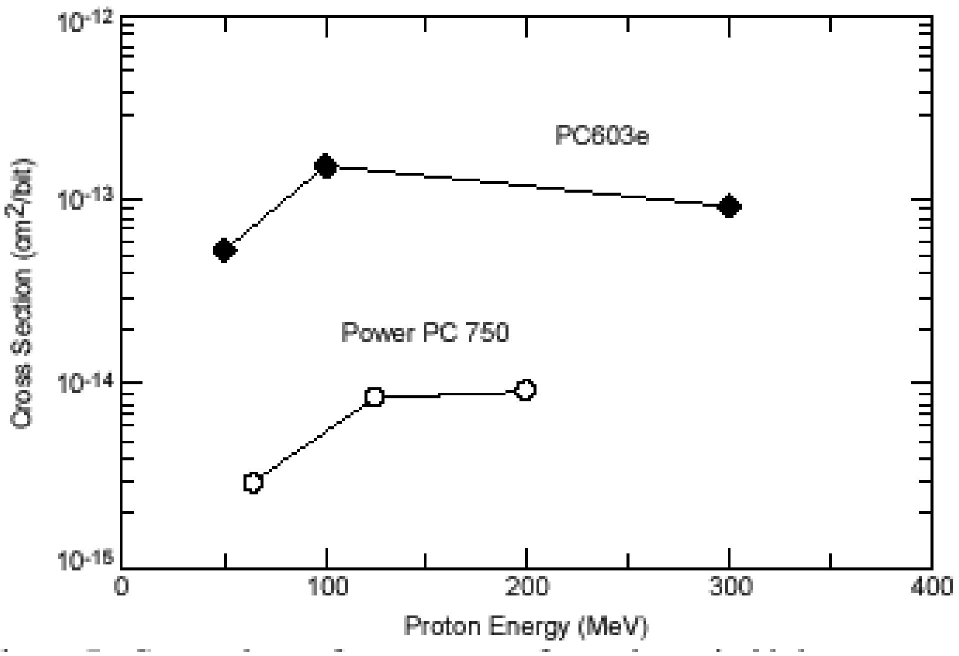
  example for old SRAM : 1.e-9/bit/h at 36 Kft : 128 Ko => SEU rate = 1.e-3/h

Scaling effect on DRAM memories



The figure beside shows how the sensitivity of Proton upset rates have changed as DRAMs have evolved. The upset rate has steadily declined, on average over several DRAM generations.
It is apparent that there are large differences in the upset rate of devices from different manufacturers. This is probably related to the design of the wells; most DRAMs use a triple-well structure in order to reduce leakage current in the memory array.

Scaling effect on PPC microprocessors



The figure shows the dependence of Proton upset cross section on Proton energy for register errors, normalized per bit, for two processors.

The threshold energy is essentially the same, but the cross section of the PPC750 processor is more than an order of magnitude lower than that of the PPC603e.

Both processors use thin epitaxial layers over highly doped substrates. The PC603e was designed with a feature size of 0.35 µm, while the feature size of the Power PC750 is 0.25 µm.

Conclusion about scaling effect

- Recent data on upset from high-energy Protons indicates that the soft-error problem in DRAMs and microprocessors is less severe for highly scaled devices, in contrast to expectations.
- Test results on processors indicate that their responses to Protons are dominated by errors in registers and in the cache memory. It is possible that faster devices may be susceptible to transient errors in logic or other regions of the processor, creating a scenario where the upset rate may increase with further scaling.
- It is impossible to predict the results for new technologies and more work would have to be done to investigate the dependencies for the more compact structures that occur in circuits.
  This would required three-dimensional simulations which are difficult to interpret because of the many variables involved.

SOI : Silicon-on-Insulator Technology

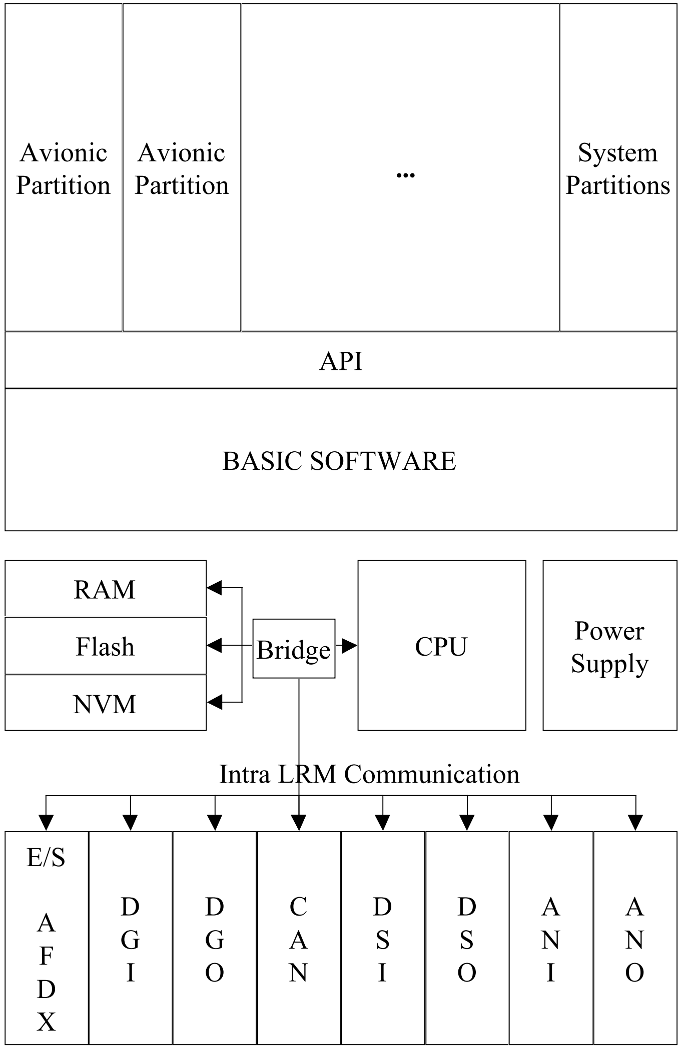
- Results for SOI processors from much older technologies indicated that the **threshold LET** was approximately five time higher for equivalent SOI structures.

  The bipolar parasitic transistor between source and drain can be turned on by heavy ions or recoil products from Protons or Neutrons, providing far more current than that due to the ionization.
- If the newer processors like IBM PPC 750 FX behave similarly, the net effect will be to reduce SEU rate in either space or terrestrial environments by about one order of magnitude.
- No radiation test results are available at this time.

Atmospheric Neutrons Effects on Avionic

Numeric example

Avionic definition : LRM architecture



IMA: Integrated Modular Avionic

- Several applications in the same LRM with different Criticality Level (A to E)
- Core Software (A653) with strong partitioning (space and time)
- Airborne Data Load (A615A)
- Ethernet Full Duplex 100FX (A664)

CPU: Design Problem / Solution

- Cost : COTS component (µP, memory)
- Throughput : RISC with cache
- Consumption : CMOS low voltage
- Obsolescence : standard PCI, PPC

Aircraft Environment

- **Eugene Normand (Boeing, 1992) :**
  - **Influence of Neutron Flux on SRAM 1 Mbit : 1.e-9/bit/h**
  - **visit www.boeing.com/assocproducts/radiationlab/publications**
- **Clive Dyer (UK DERA) : detectors in Concorde Supersonic**
- **ABD100.1.2 (issue D) Environment §4 : Atmospheric Radiation Environment**
  - **The continuous increase in integration of electronic devices, and the flight altitude and latitude of new aircraft, need radiation to be considered for safety-reliability-availability of related aircraft functions.**
  - **Normalisation : Altitude 40Kft, Latitude 40°N :**
    0.89 neutron/cm^2.s in the range 1-10 MeV
  - **Single Aisle : Fluence (1-1000 MeV) (1 fh) = 5.e3/cm^2 => 1.4 n/cm^2.s**
  - **Long Range : Fluence (1-1000 MeV) (8 fh) = 7.e4/cm^2 => 2.4 n/cm^2.s**

=>mean value (tbc) : 1 n/cm^2.s = 3600 n/cm^2.h

(pessimistic Avionic/SE(*2), LET threshold > 10 MeV ?)

ABD100.1.9 (issue D) : Electronic §2.4 SEU Related Implementation Requirements

- The hardware and software implementation solutions shall consider the possibility of SEU (Single Event Upset) due to particle environment (radiations as for example: neutrons, protons, heavy ions, etc.) at high flight altitude
- The LRU availability requirements (MTBF/MTBUR) and safety requirements (occurrence rate of undesired events) shall be met, taking into account the SEU risk.
  - Mean Time Between Failures /MTB Unscheduled Removal
  - NFF(No Fault Found) < 15%

- Assess the risk on RAM, registers of µprocessor & EPLD.
- Ensure any IC packaging is not a source of high energy particles

Examples of Hardware Specification

- **SEU and MEU consequences shall be considered in the Safety analysis and relevant precautions shall be included in the design (impact < 10% MTBUR)**
- **LRM undetected erroneous behaviour < 1.e-5/fh**
- **Bus_in-CPU-Bus_out undetected failure < 2.e-6/fh**
- **undetected failure (objective)**
  - **CPU < 1.e-6/fh**
  - **Bus < 1.e-7/fh**
  - **… (without SEU/MEU effects : figures to be provided)**
- **NFF < 15%**

Examples of Software Specification

- The CPM memory allocation function shall provide memory partitioning : segregation mechanisms shall prohibit memory access Read, Write and Execute, outside the memory area of the current running partition.
- The CPM shall ensure that a partition behaving erroneously (e.g. because of a software bug) cannot jeopardise function or performance of other hosted partitions nor of Core Software
- The Basic Software shall not be able to corrupt partitions code

Example choices

- **Main memory SDRAM 256 Mbits : up to 256 Mo**
  Micron MT48LC16M16 (16M16bits) (CMOS 3.3V)
- **Bridge ASIC or CPLD :**
  Altera EP20K600E (CMOS 1.8V 0.15µ 600Kgates)
- **µprocessor PowerPC :**
  IBM PPC750CXe (CMOS 1.8V 0.18µ copper)
  - **processor clock 400 MHz**
  - **internal cache L2 (256Ko) with ECC**
  - **cache L1 data (2*32Ko) no parity**
  - **cache L1 tag (2*128 tags 4 way 20 bits) no parity**
  - **MMU TLB (2*128 PTE 64bits) no parity**

Hypothèses Générales SEU / MBU

- L'effet des neutrons atmosphériques est comparable à celui des protons pour les énergies > 50 MeV
- Pas de phénomène de latchup avec les neutrons (aujourd'hui)
- Il est acquis qu 'il existe des MBU provoqués par des protons (1% des SEU observés dans des essais SDRAM)
- L 'effet est très dépendant de la technologie y compris au changement de masque pour un même fabricant (problème des obsolescences)
- Les mémoires FlashPROM sont peu sensibles en lecture (tbc)
- Le principal problème concerne la SDRAM vu sa taille : 128 Mo = 1 Gbit
- La sensibilité dépend du taux d 'utilisation par le logiciel (duty cycle), en particulier pour les caches du microprocesseur ou les FIFO d 'un automate DMA (ratio statique / dynamique)

SDRAM

- Données chiffrées d ’essais sur SDRAM 256 Mbits Samsung K4S560432A-TC75 montrent une section efficace (protons) : σ = 3.e-16 cm_ /bit.

  Donc pour un flux de 1neutron /cm_.s = 3600 n/cm_.h :

  Le taux de SEU est de => 10^{-12} / bit. h

  Pour 128 Mo = 1 Gbits => **10^{-3} / h** >> objectif 10^{-6} / h

  En prenant MBU = 1 % de SEU => 10^{-5} / h > objectif 10^{-6} / h

  ==> Code correcteur multi-bit obligatoire (e.g. Reed-Solomon)
- Ratio statique / dynamique pas significatif pour la mémoire SDRAM
- Il existe des MBU ayant un effet « bloquant » du composant (SEFI) (e.g. l ’automate de self-refresh) dont on ne sort que par coupure de l ’alimentation

  => LRM Reset externe avec cycle coupure alimentation (pour la disponibilité)

FPGA & CPLD

- FPGA Antifuse QuickLogic : très bonne tenue
- FPGA EEPROM Actel ou Altera Max7000 : bonne tenue
- SRAM CPLD Xilinx : très sensible => redondance & rechargement
- Altera APEX (CPLD SRAM pour maquette, puis version MPLD masquée) :
  données ALTERA en essai neutron sol (25 n/cm_.h) (JESD89 ?) :
  EP20K400E (16640 LE) : 1.9 e-6 /h (sol) => 2.7 e-4/h (40 Kft) (*144) => **MPLD**
  user memory : 3.7 e-13 /bit.h (sol) => **σ = 1.47 e-14 cm_/bit**
  =>SEU rate = 5.3 e-11 /bit.h (40 Kft) (*144) => FIFO duty cycle ratio

➡ **Précautions de design au niveau VHDL**

- Codes correcteurs pour registres « statiques »

- Parité pour détection

- Redondances (A bon escient !)

- ...

PowerPC 750CXe Architecture

Instruction Unit
Fetcher Branch Processing
Inst. Queue (6) BTIC (64)
Dispatcher

Inst.MMU
IBAT (4*2)
SR (16 shadow)
ITLB(128)

I Cache
32 Ko
Tags (128*8)

IU 1

IU 2

System Register

GPR
32 bits
(32 + 6)

Load / Store Unit
EA
Store Queue

FPR
64 bits
(32 + 6)

FPU
FPSCR

Completion unit
Reorder (6)

Data MMU
DBAT (4*2)
Seg. Reg (16)
DTLB (128)

D Cache
32 Ko
Tags (128*8)

60x Bus I/F
Fetch Queue
Load Queue
Castout (2)

L2 Cache
256 Ko + ECC
Tags (2048*2)
L2CR

PPC 750 (1)

- Il existe des essais sur PPC 603 (CNES) et sur PPC 750 (NASA)
- Les résultats du PPC 603 (0.35µ) et du PPC 750 (0.25µ) ne sont pas immédiatement transposables au PPC 750CXe IBM (0.18µ)
- Le **PPC 750 CXe** (IBM) a l 'avantage d 'avoir un **cache L2 interne avec ECC** de détection d 'erreur sur 2 bits (exception Machine Check) => reprise à chaud

→ **fonctionner en mode write through pour cache L2**

- Les principaux problèmes concernent le **cache L1 et la MMU**
- Le ratio statique / dynamique est de l 'ordre de 10, mais sans confirmation expérimentale très fiable car très dépendant du logiciel de l 'application.

  Possibilité de faire des essais sur un benchmark en simulation logicielle d 'upset (**CEU** : Code emulating an upset => TIMA Grenoble)

PPC 750 (2)

- Ordre de grandeur pour PPC 603P (2.5V 25MHz) (données proton CNES)
  - Mesure en statique σ = 4.4 e-14 cm_/bit flux = 3600 n/cm^2/h
  - Cache data L1 = 16 Ko = 128 Kbits -> 4.3e-5 /h
  - ratio FFTcache / FFTnocache = 1.5 (ion lourd) (no effect = 42%)
  - Si ratio statique/dynamique = 1/10 -> 4.3e-6 / h
- On cherche < 10^{-6} /h, d 'où l 'importance de la mesure en statique et du ratio statique/dynamique pour les caches
- =>Confirmer le passage des mesures protons à neutrons
  (section efficace à saturation & valeur du LET seuil)
- =>Sensibilité des caches = 50% registres (IEEE TNS dec01) ?
- =>Trouver une méthode pour évaluer le temps de risque dans les caches à partir du taux de cache-miss et du mode copy-back / write-through !

PPC 750 (3)

- **IEEE TNS Vol.48 No.6 décembre 01(G.Swift et al NASA/JPL)**
  « Single Event Upset in the PowerPC750 Microprocessor »
  Proton static register cross section :

XPC750 Motorola (2.5V 0.29µ)	**σ = 1.2 e-13 cm_/bit**
PPC750 IBM (2.5V 0.26µ)	**σ = 1.0 e-13 cm_/bit**

- **PowerPC 750CXe (1.8V 0.18µ)** **σ = ?**
  (σ = 1.0 e-13 cm_/bit & flux = 3600 n/ cm_/h **=> 3.6e-10 /bit.h)**

Instruction registers :	**672 bits**		**=> 2.5e-7 /h**
Data registers (GPR+FPR) :	**3264 bits**		**=> 1.2e-6 /h**
Instruction L1 cache :	**32 Ko**		**=> 9.4e-5 /h**
Data L1 cache :	**32 Ko**		**=> 9.4e-5 /h**
L2 cache :	**256 Ko**	→	**ECC (64+8bit)**

- **Pondération par le duty cycle pour les caches et par la criticité des données de l 'OS ou de l 'application.**

PPC 750 (4)

- PowerPC 750 MMU & cache tag => adresse physique
  événement redouté : écriture erronée dans une autre partition
  - D TLB : 128 PTE 64 bit => 8192 bit
    4 DBAT 64 bit => 256 bit
  - L1 Dcache tag : 128 tags 8 way 20 bit PA[0-19] => 20480 bit
    L2 cache tag : 4096 tags 2 way 20 bit => 163840 bit
  - Total : 200 Kbit (physical address for translation)
  - duty ratio (30%) (write only) => 1.e-10 /bit.h
  - => écriture à une adresse erronée : 2.e-5/h
- Trouver toutes les failles de propagation des fautes à travers la MMU et les caches vers les autres partitions.
- Protéger les accès « write » dans le bridge mémoire en fonction de la partition courante.

Conclusion

- **Mémoire SDRAM protégée par EDC (Reed Solomon) et fenêtres écriture**
- **Problème avec les caches du PowerPC 750**
  - **Instruction : détection par deadline, watchdog -> 1.e-6 /h (99%?)**
  - **Cache data L1 : difficile à détecter -> 9.e-5 /h**
  - **Ratio statique/dynamique -> 5.e-5 /h (50% no effect ?)**
  - **Feature size : (0.18µ/0.26µ)^2=0.4 -> 2.e-5 /h**
    mais tension 1.8V au lieu de 2.5V
- **On cherche «erroné non détecté CPU» < 10^{-6} /h, d 'où l 'importance de la mesure en statique et du ratio statique/dynamique pour les caches**
- **Duty cycle est fonction du cache miss et du mode de fonctionnement du cache (copy back / write through) (effet sur la performance)**
- **Futur PowerPC750Fx (SOI) avec parité sur cache L1 et tags**

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  www.SRIM.org Ziegler's papers

Axes d’étude (matériel et logiciel)

- Confirmer le passage proton -> neutron (taux MBU, LET seuil)
- Mesures sur PPC750CXe (IBM) et MPC755 (Motorola)
- Mesures sur PPC750FX (Silicon On Insulator)
- Sensibilité cache / registre du microprocesseur
- Ratio de sensibilité statique /dynamique (duty cycle) sur des benchmarks représentatifs

- Simulation d ’upset par logiciel (CEU)
- Recherche des variables critiques d ’un logiciel
- AEEL : analyse des effets des erreurs logicielles
- Règles « Defensive Programming »
- Redondance logicielle rapide