

# Génération de fautes par impulsions optiques dans les circuits intégrés. Etude de la SdF des systèmes complexes embarqués

J.H. Collet<sup>(1)</sup>, F. Sellaye<sup>(1)</sup>, J.F. Pascal<sup>(2)</sup>, F.X. Guerre<sup>(2)</sup>, G. Rouxell<sup>(3)</sup>

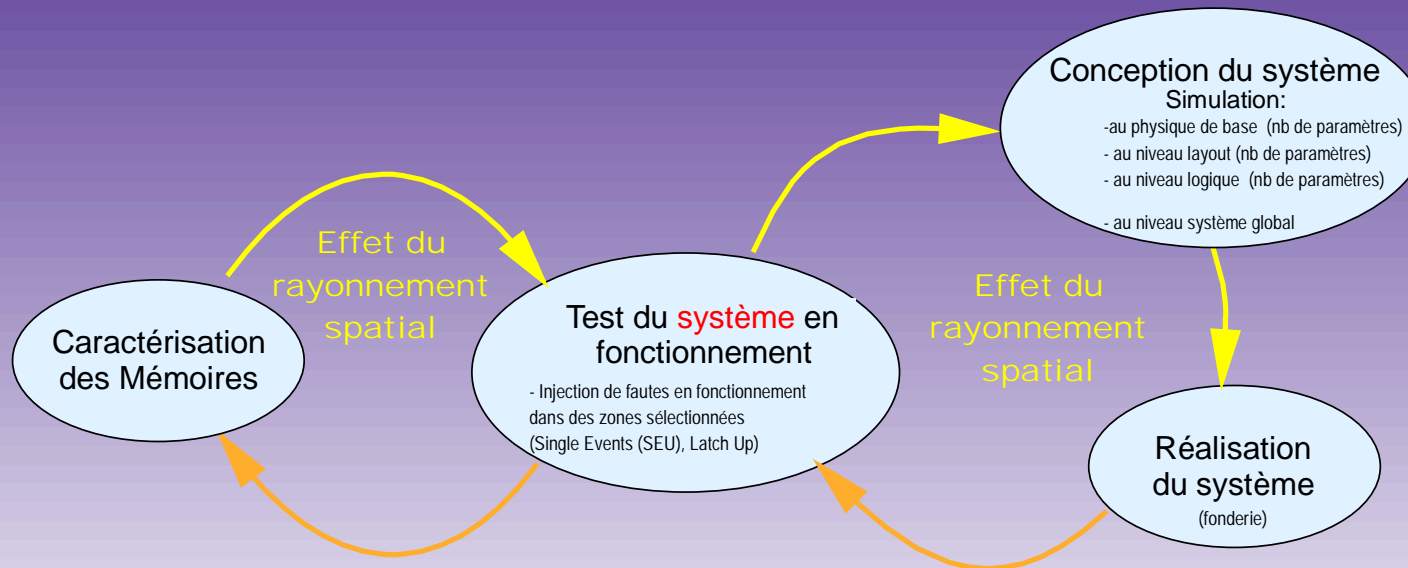
(1) Laboratoire d'Analyse et d'Architecture des Systèmes du CNRS  
7 av. du colonel Roche, 31077 Toulouse FRANCE

(2) Hirex Engineering, 117 rue de la Providence  
31500 Toulouse FRANCE

(3) TEMIX MHS, La chanterie  
route de Gachet, CP 3008, 44087 Nantes CEDEX 03, FRANCE

***LAAS-CNRS 7 av. du colonel Roche Toulouse 31000***

# Intérêt des tests sous irradiation laser dans la conception et la réalisation des systèmes électroniques complexes embarqués?



# Mémoire Dynamique 64 MB

Device: SAMSUNG SDRAM  
64 Mb KM41654030 CT G8

## Physical organization

64 Mb= 16x16 blocks of 256kb

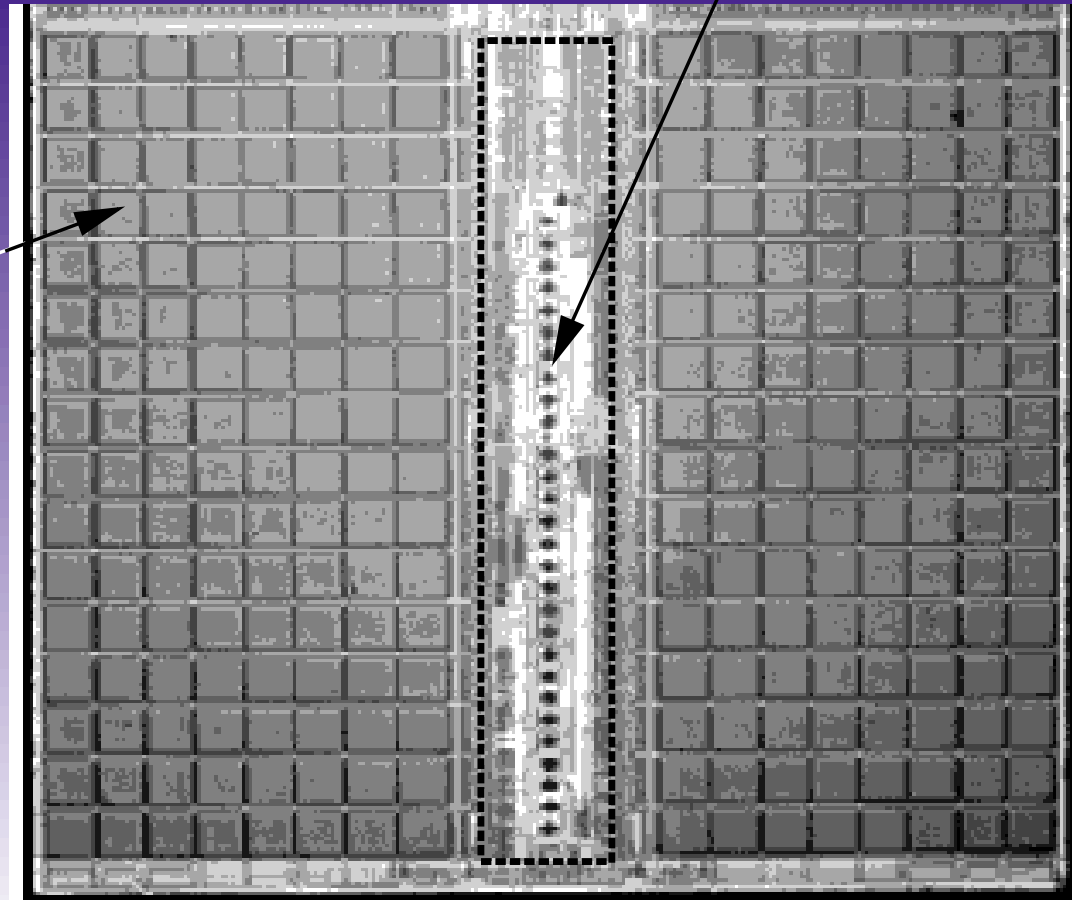
## Logical organization

64 Mb= 4 bancs or 1Mb addresses with  
2 bytes/address

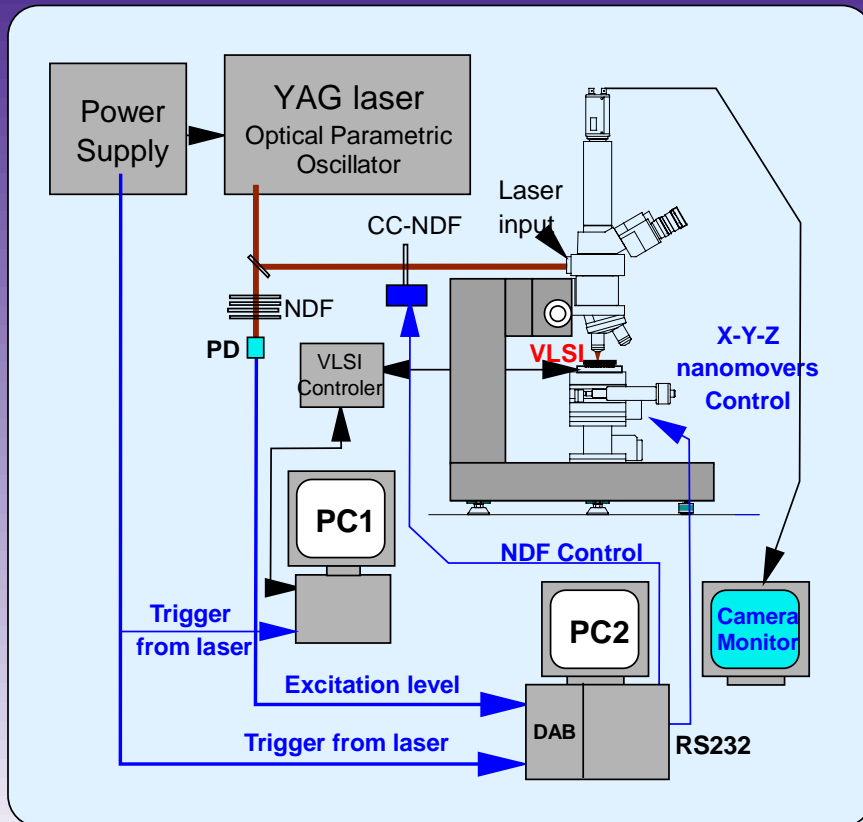
each address: 2 bits for bank

12 bits for row

8 bits for column

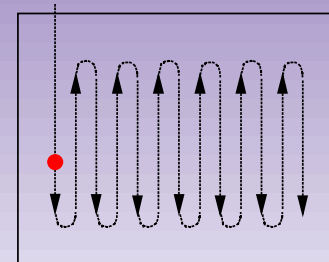


# Facilities for picosecond irradiation of Silicon



## main features:

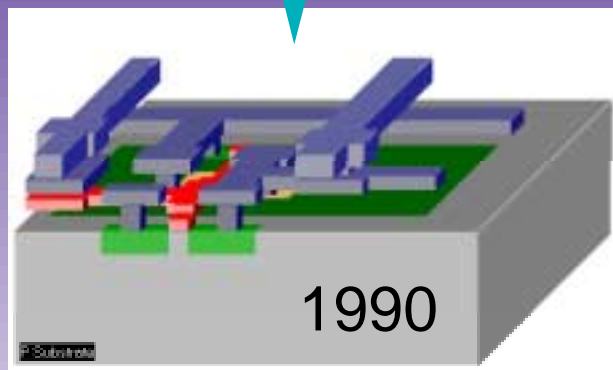
- Adjustable excitation wavelength
- Picosecond pulses at 10 Hz
- Spot size slightly less than  $0.5 \mu\text{m}$
- Automatic scanning and recording



## *Front irradiation versus Back Irradiation*

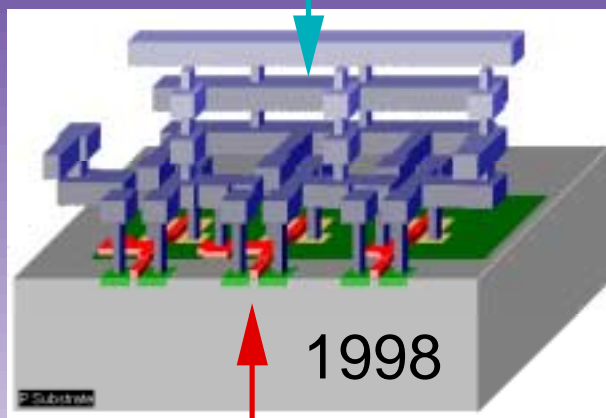
Front Irradiation

2 metal layers



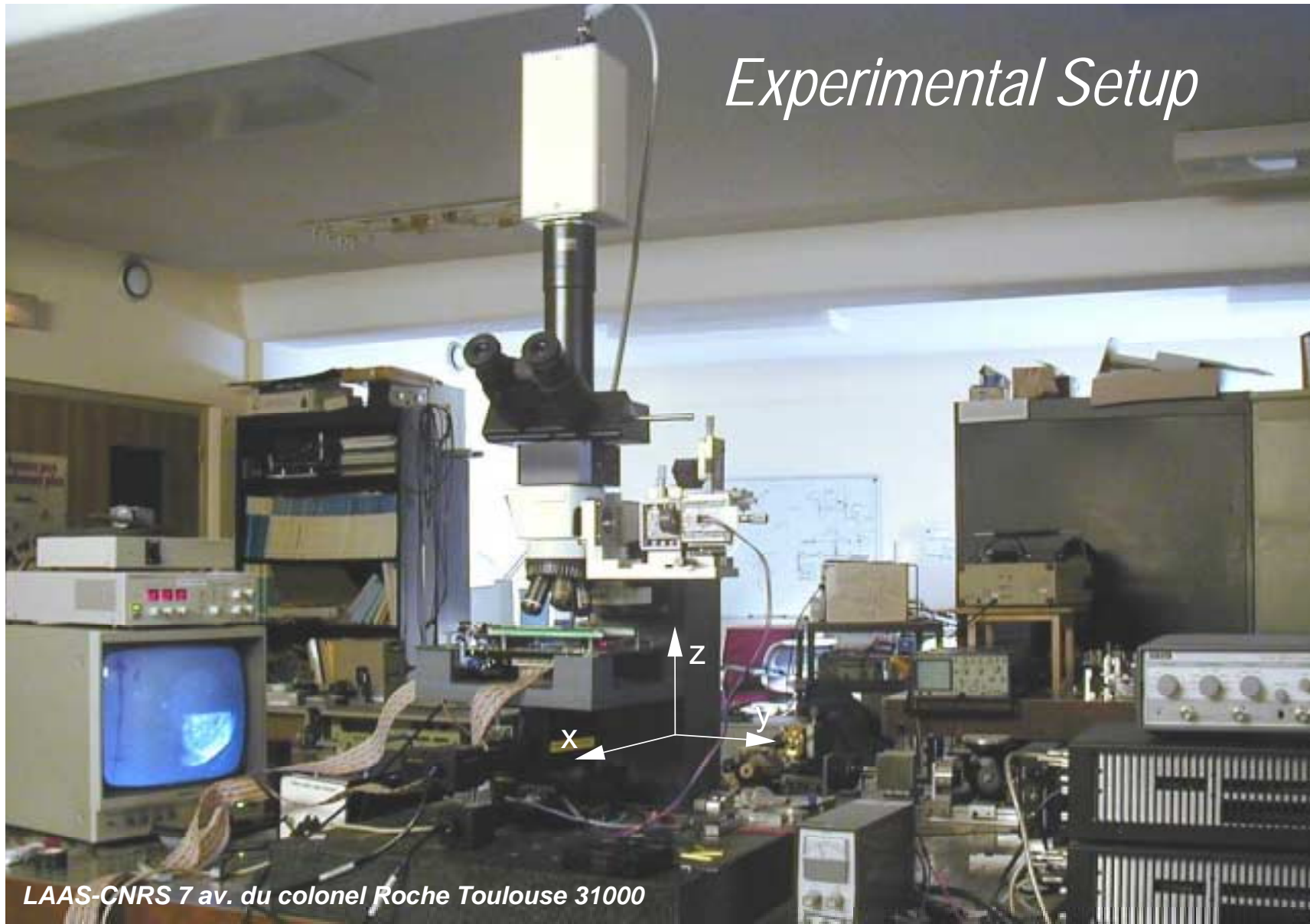
Back Irradiation

4 metal layers



**Back Excitation**

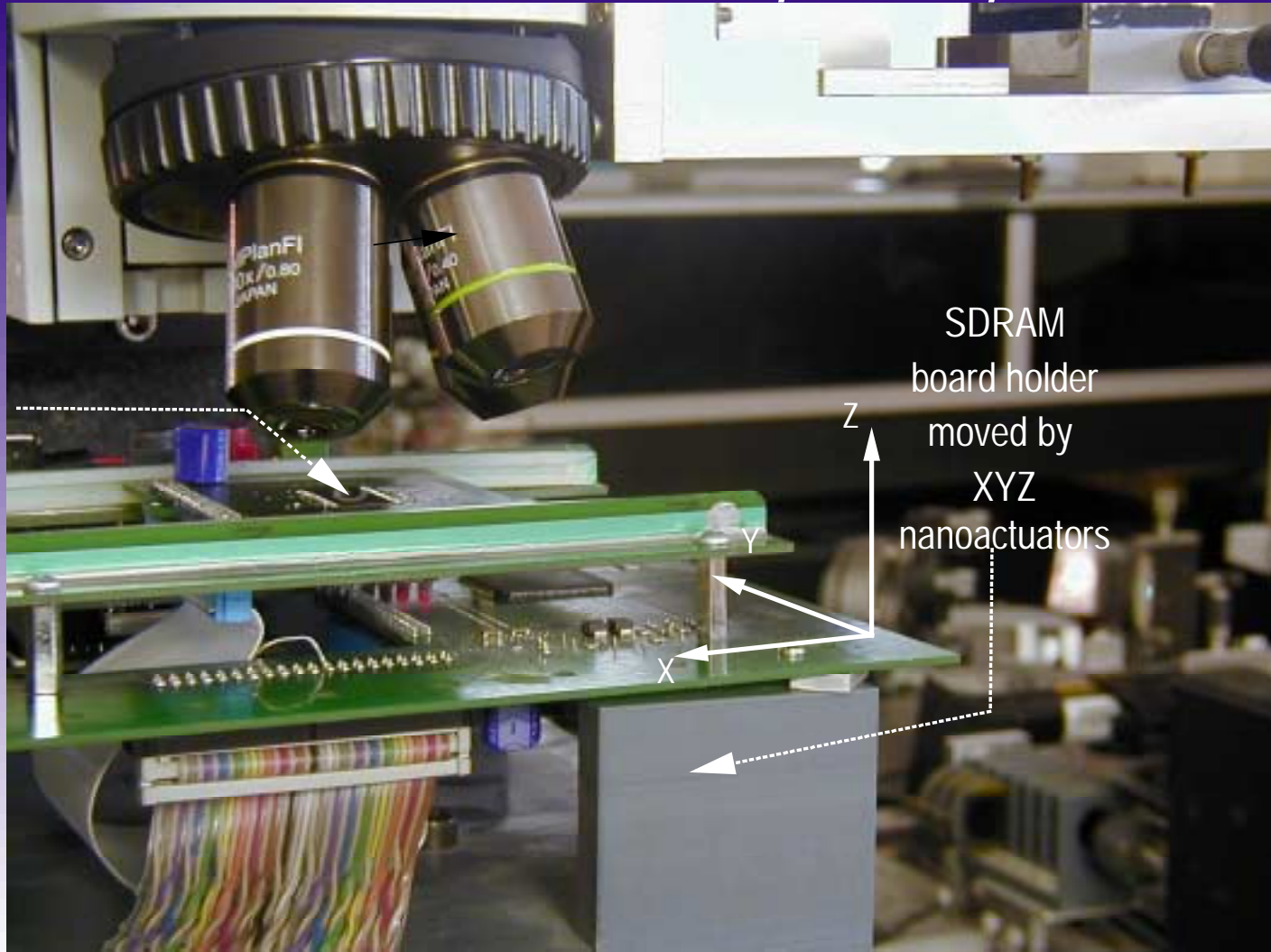
# *Experimental Setup*



LAAS-CNRS 7 av. du colonel Roche Toulouse 31000

## *RAM holder and microscope setup*

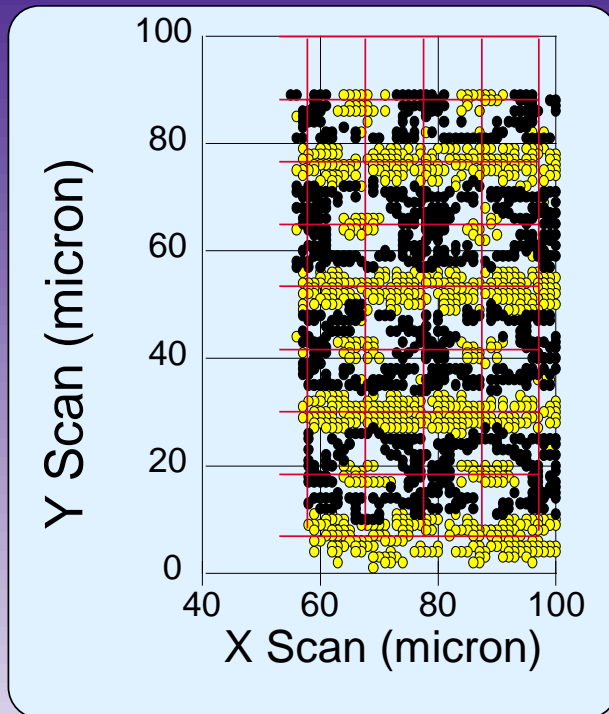
polished  
flip-chip  
SDRAM



SDRAM  
board holder  
moved by  
XYZ  
nanoactuators

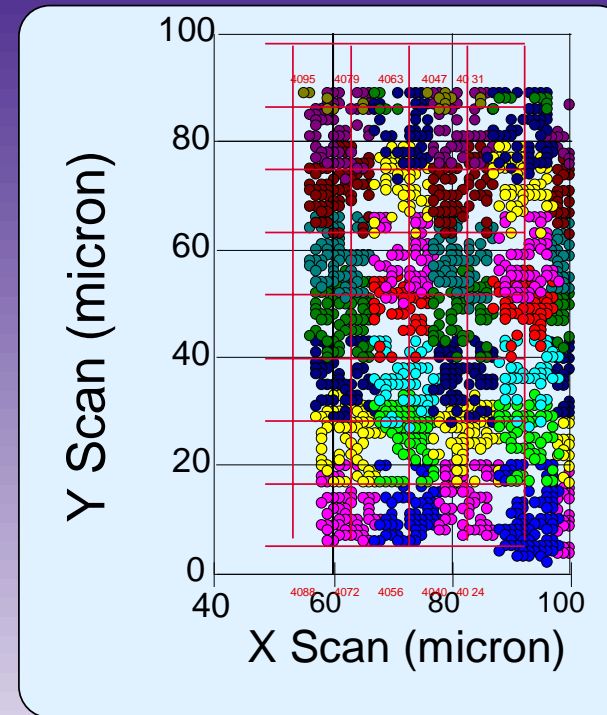
# Front excitation: 1- $\mu\text{m}$ -step SEU Map

Dual-port SRAM 67025 Temic



Yellow point: 1 memory bit switched from 0 to 1

Black point: 1 memory bit switched from 1 to 0



Incident energy: around 0.3 nJ

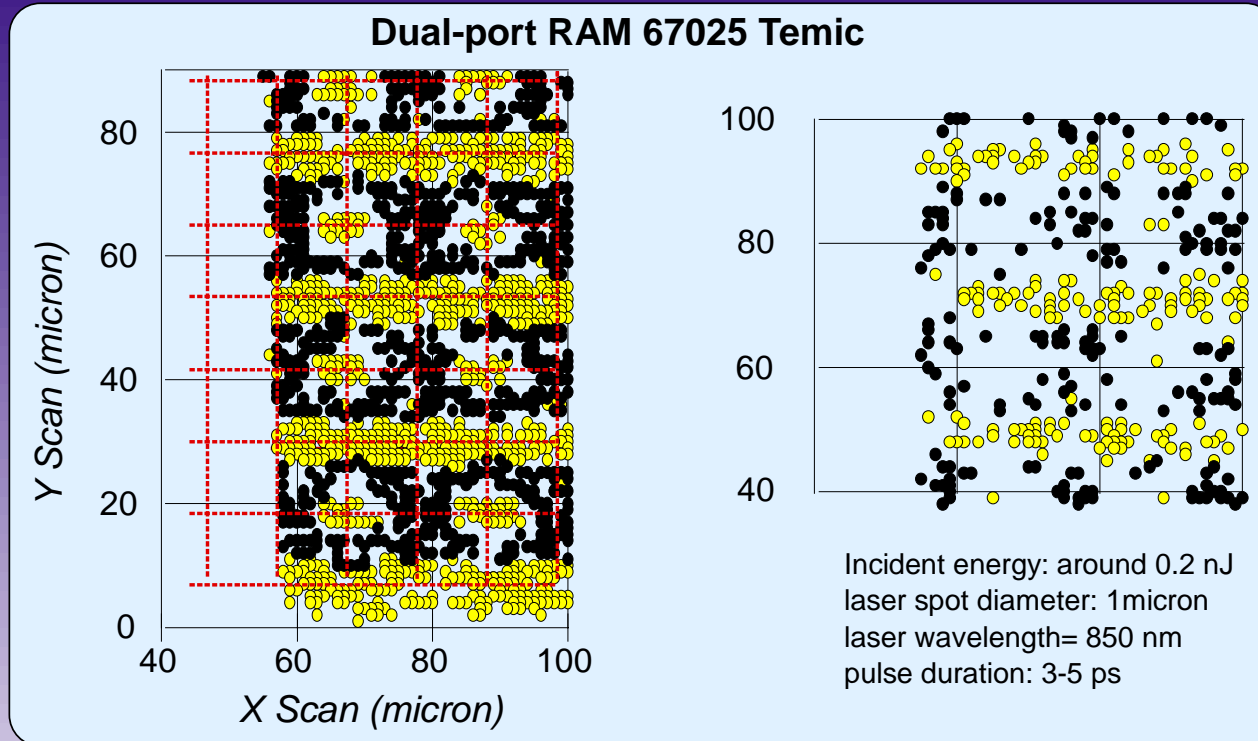
laser spot diameter: 1 micron

laser wavelength= 850 nm

pulse duration: 3-5 ps

**LAAS-CNRS 7 av. du colonel Roche Toulouse 31000**

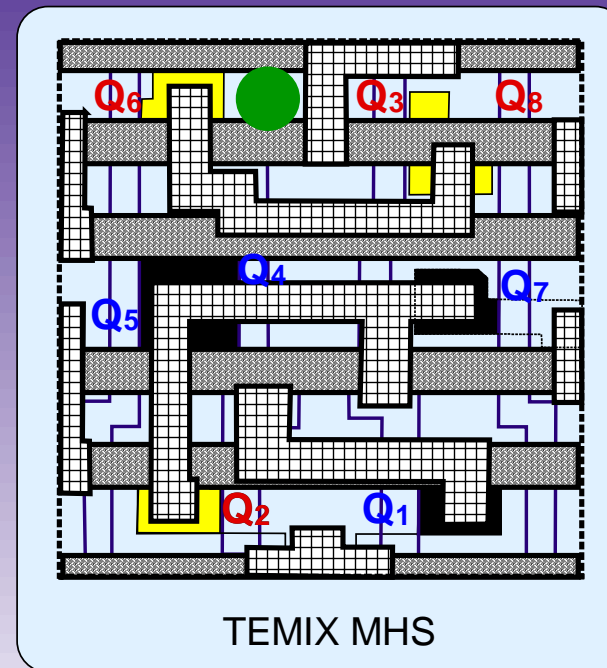
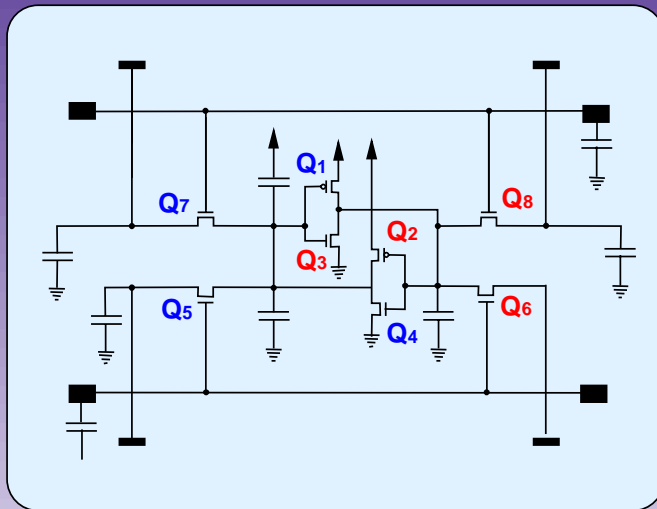
# 1- $\mu\text{m}$ step Mapping of SEU's: Threshold energy

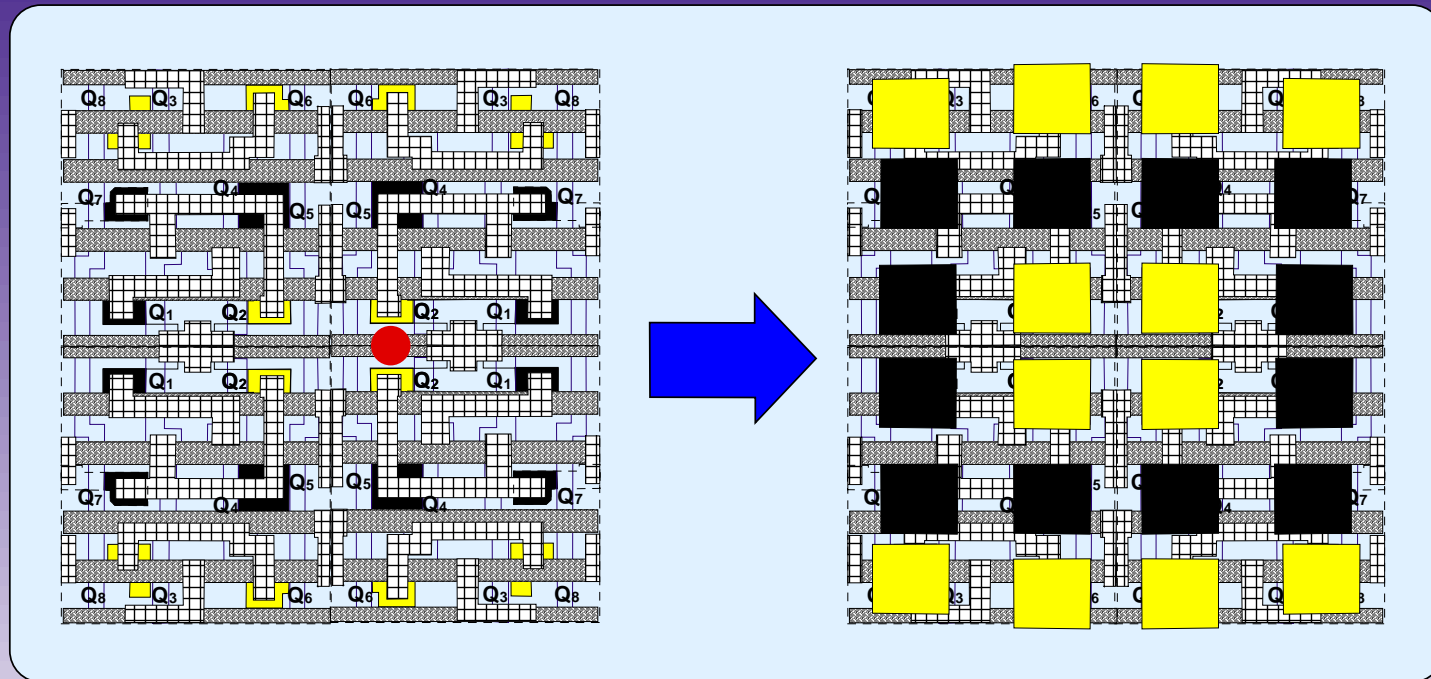


$$N_o = E_p T / h\nu$$

$N_o = (2.5-5) \times 10^8$  EHP's are photocreated with pulse energies ranging from 0.1 to 0.2 nJ. However:  $N_P = (1-3) \times 10^7$

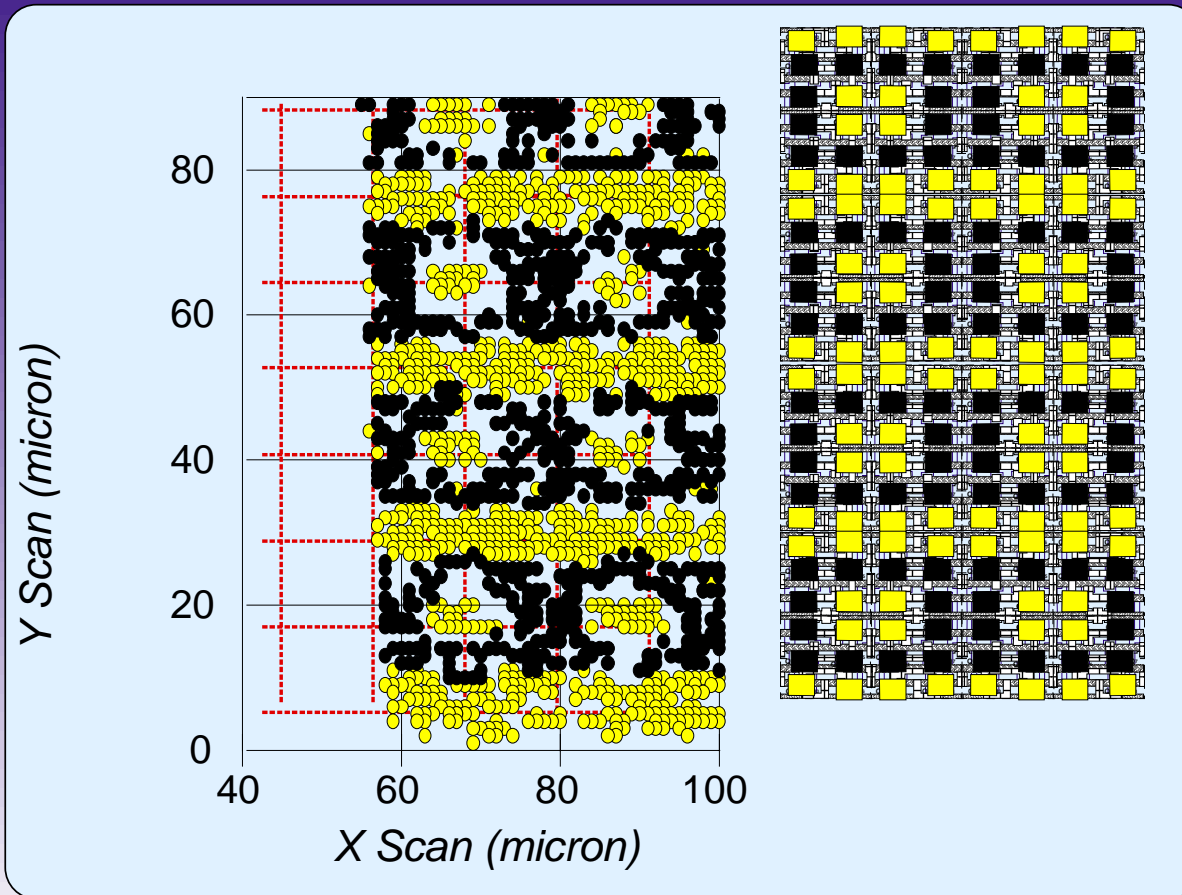
# Comparison with the chip layout and identification of sensitive nodes





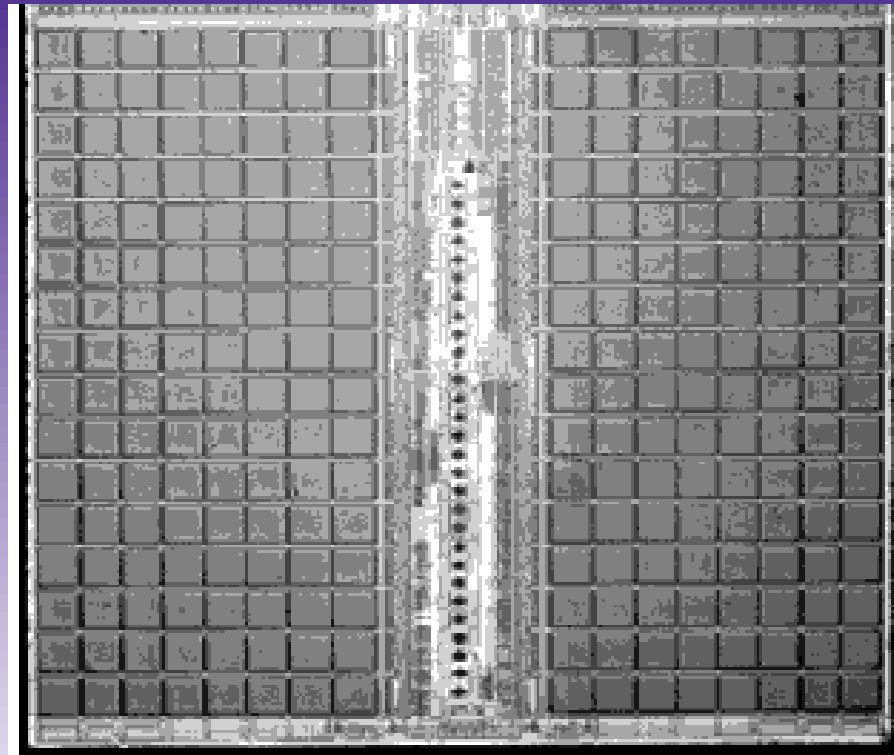
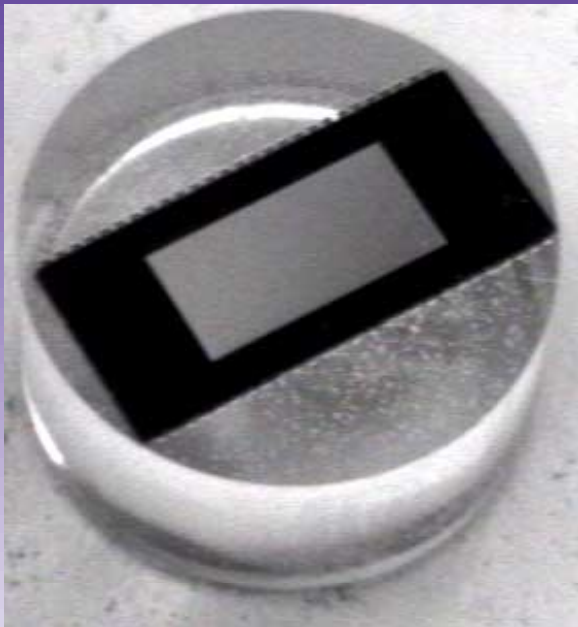
LAAS-CNRS 7 av. du colonel Roche Toulouse 31000

# Comparison of SEU mapping with the chip layout



# *SDRAM substrate polishing*

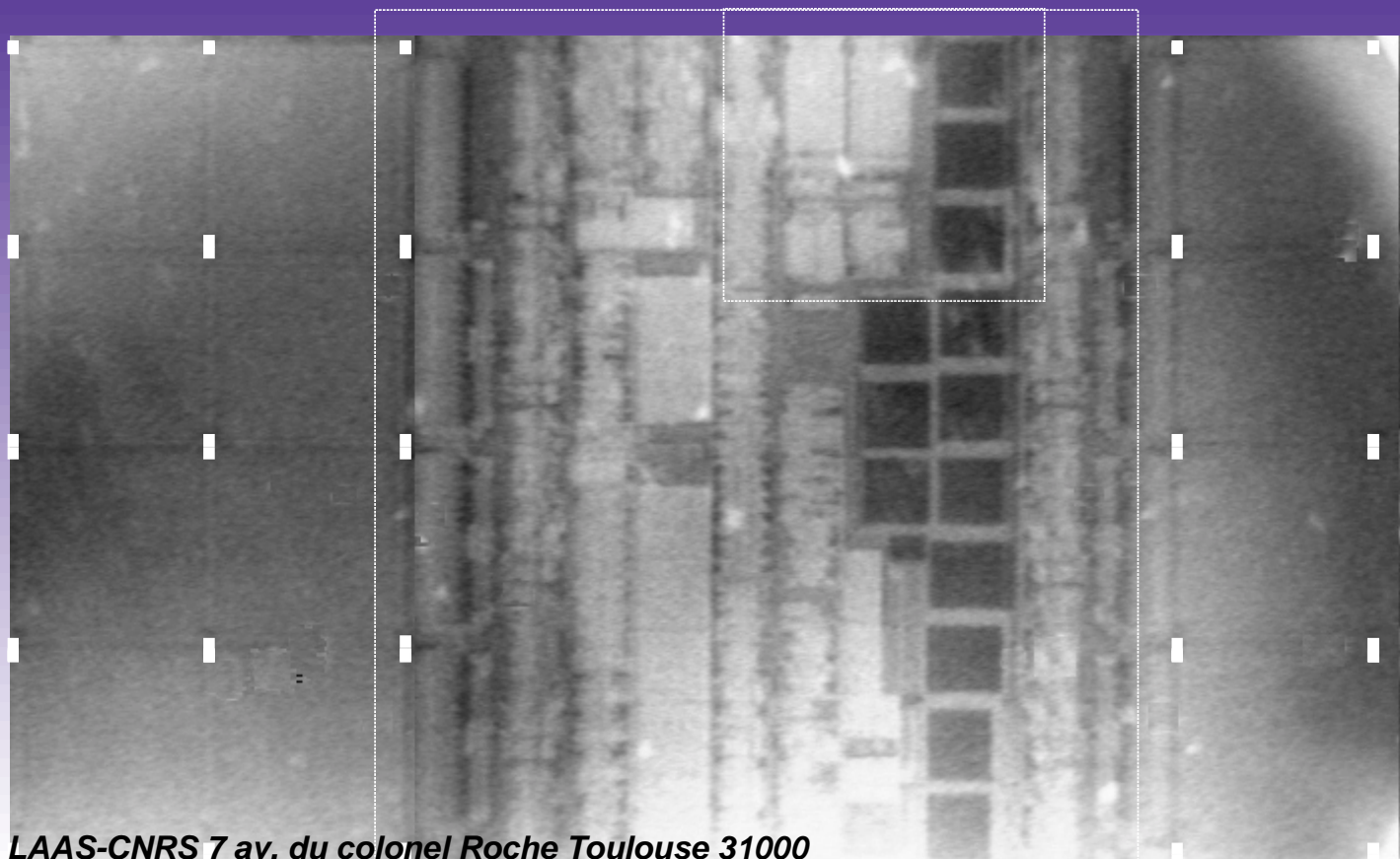
Device: SAMSUNG SDRAM  
64 Mb KM41654030 CT G8



# *Infrared Imaging through the back side*

Lens x5, NA=0.15

300  $\mu\text{m}$



**LAAS-CNRS 7 av. du colonel Roche Toulouse 31000**

# Processeur

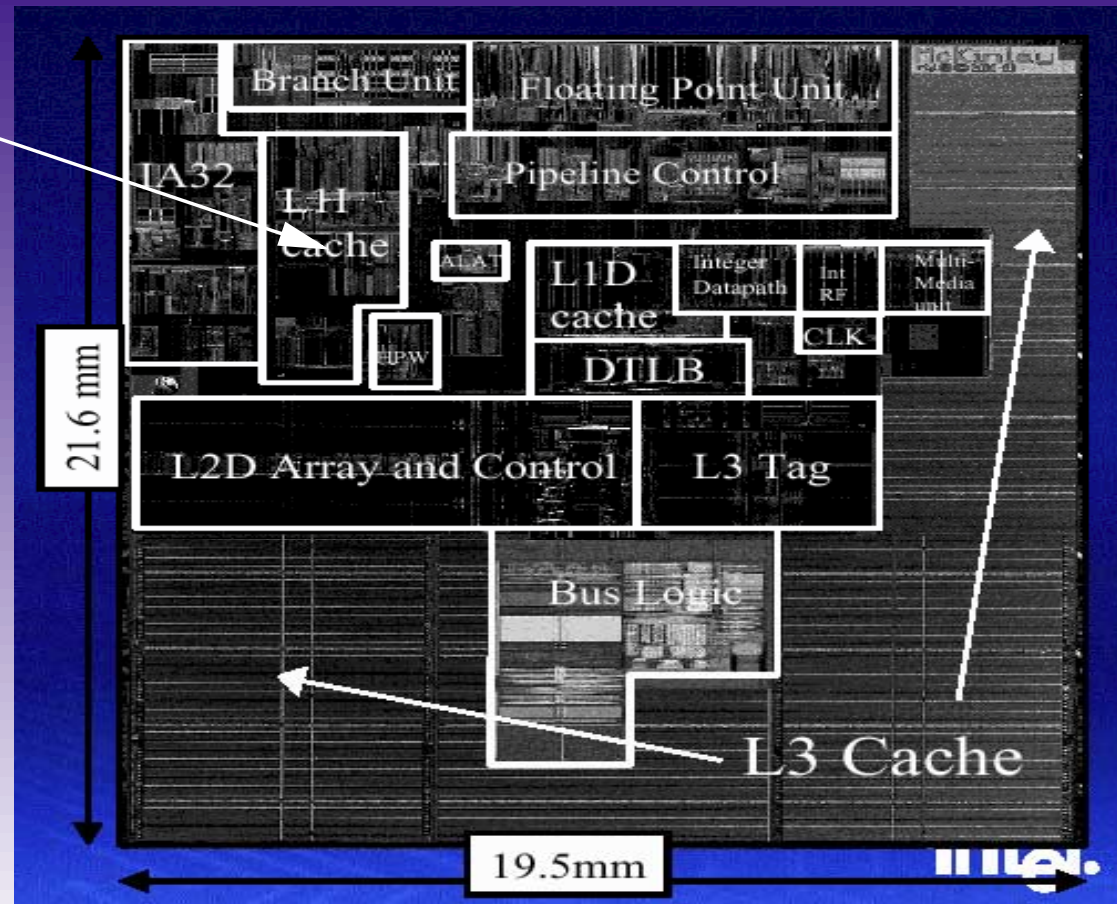
Que se passe-t-il si une faute est générée ici?

## Itanium 2

- .18  $\mu\text{m}$  bulk, 6 layer Al process
- 8 stage, fully stalled in-order pipeline
- Symmetric six integer-issue design
- IA32 execution engine integrated
- 3 levels of cache on-die totaling 3.3MB

• 221 Millions total transistors

• 130W @1GHz, 1.5V  
(source: INTEL)



# *Conclusion*

- 1) Les techniques d'excitation optiques permettent d'irradier précisément des zones de systèmes complexes (Processeur: cache, registres, pipeline d'un processeur, logique de prédiction de branchement, etc..) (DRAM: Logique de contrôle, zone mémoire..)
- 2) On peut tester dans un cycle de validation de systèmes complexes (system on chip) la sensibilité des différentes composants au rayonnement etc...)