Principles of Radiation Hardening by Design: The Case of LEON

Atelier Technicatome
Réseau d'Ingeniérie de la Sureté de fonctionnement
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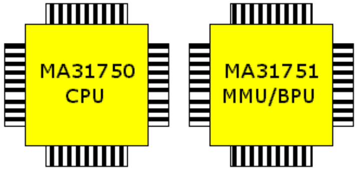
Overview of ESA Microprocessors

beg 90’s

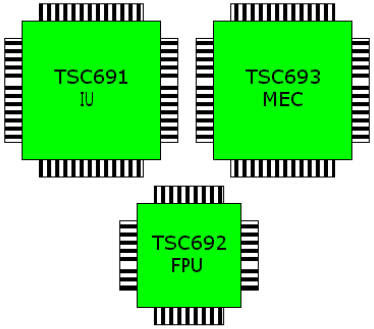
MA31750



- MIL-STD-1750, 16 bit
- CSIC (microcoded)
- Two chips
- 84 and 68 pins
- 2 MIPS at 16 MHz
- Designed and manufactured by GPS
- CMOS/SOS 1.25 micron
- Full European design
- Largely sold and used in Europe, in USA and other countries
- Still under production at DYNEX Semiconductor

mid 90’s

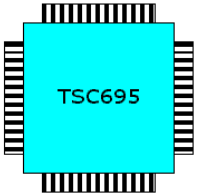
ERC32 3-chip set



- SPARC V7, 32 bit
- RISC
- Three chips
- 256, 160, and 256 pins
- 10 MIPS at 14 MHz
- Manufactured by TEMIC
- CMOS RT 0.8 micron
- Partial European design
- Used in man space systems: DMS-R, SPLC, ERA, ATV, and also in PROBA
- Phase-out: Last buy June 2002

mid 90’s

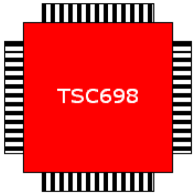
ERC32 Single Chip



- SPARC V7, 32 bit
- RISC
- Single chips of 256 pins
- 14 MIPS at 20 MHz
- Manufactured by TEMIC
- SCMOS RT Plus 0.5 micron
- Merging of the ERC32 3-chip set
- Removing of unused functions
- Addition of new functions and bug fixes

beg 00’s

LEON



- SPARC V8, 32 bit
- RISC
- Single Chip, 256 pins
- 100 MIPS
- Use of Instruction and Data caches
- LEON core designed by ESA

LEON Main Objectives

- ☐ Provide an European source of high performance microprocessor for space applications
- ☐ 100 MIPS and 20 MFLOPS target
- ☐ Shall be compatible with previous ERC32 generations
- ☐ The design shall be made in VHDL
- ☐ LEON shall be SEU tolerant by design
- ☐ The SEU tolerance shall be software transparent
- ☐ The design shall be portable
- ☐ The processor implementation should allow be reusable in system-on-a-chip (SOC) designs
- ☐ The processor should have standardized interfaces to simplify system integration and to reuse commercial cores, components, and tools.

Summary of the Specification of LEON

- ☐ SPARC V8 architecture
- ☐ Single chip (256 pins)
- ☐ 120 MHz clock operation
- ☐ Instruction and Data caches (8 Kbytes each)
- ☐ Hardware Multiplier and Divider
- ☐ FPU (SUN/MEIKO, not pipe-lined, serial I/F)
- ☐ AMBA bus (AHB and APB)
- ☐ PCI bus (33 MHz) Controller and Arbiter

Some Design Features of LEON

❑ 5-stage pipeline

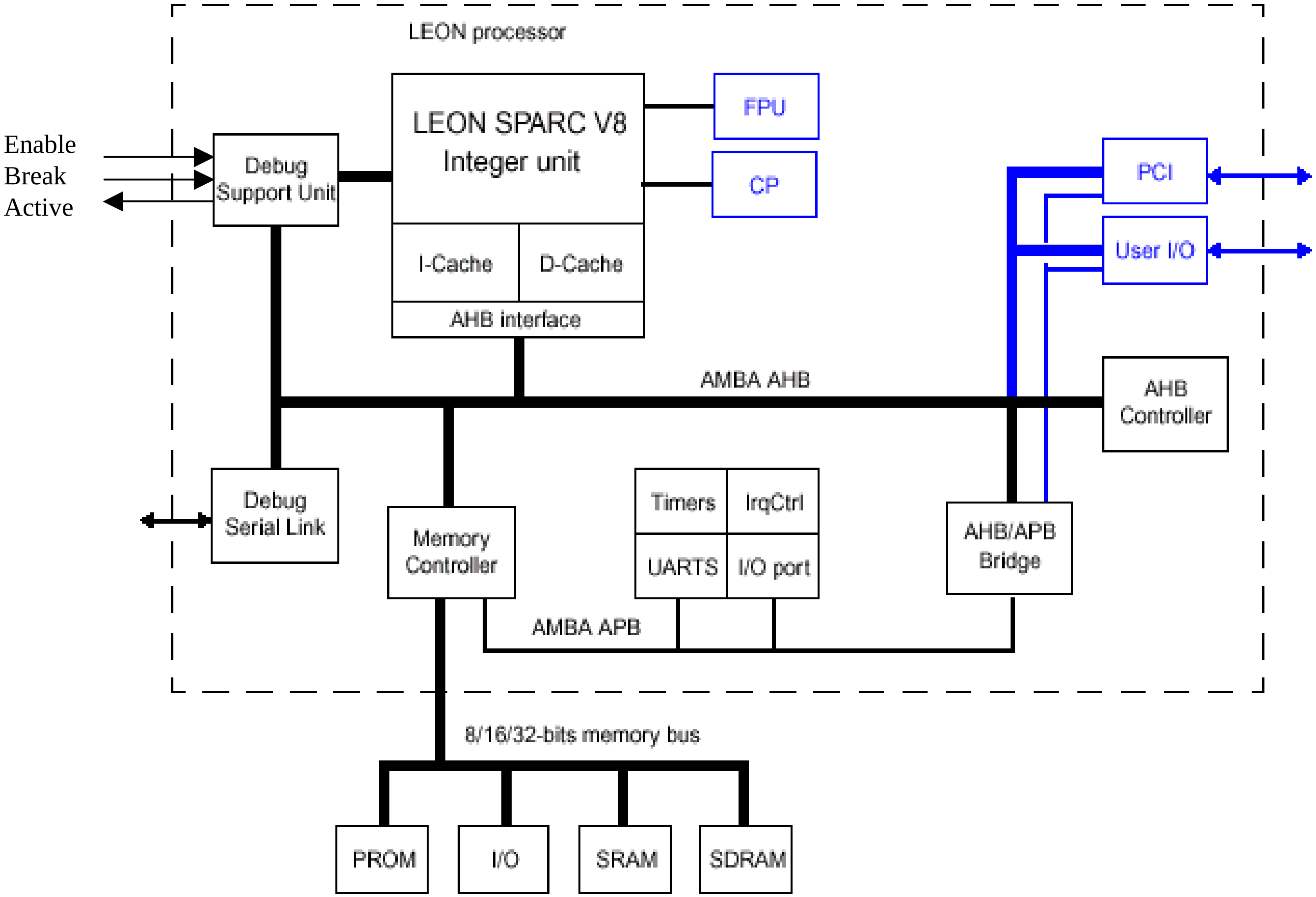
A high-speed AMBA/AHB bus is used for data transfer between the caches and the external memory controller

❑ A low-speed AMBA/APB bus is used to attach on-chip simpler peripherals such as timers, uarts, interrupt controller and I/O ports

❑ A Debug Support Unit provides debug facilities such as:

- Breakpoints
- Step by step execution
- It provides access to all registers, caches, etc …
- Synchronization with a Software Validation Facility
- Use a dedicated UART
- Trace buffer for instructions, data, and AMBA bus
- Support SVF

LEON Block Diagram



Principal Space Radiation Effects

☐ Total Ionizing Dose

- o significant increase of the power consumption
- o permanent loss of functionalities

☐ Single Event Effects

- Latch-up
  - o temporary or permanent loss of functionalities
  - o very large increase of the power consumption
  - o may be destructive
  - o a special protection circuit is required if the device is not LU free
- SEU
  - o temporary loss of correct functionalities
  - o may result in a permanent loss of correct functionalities if not detected and corrected

Brief Status of the Radiation Hardness of CMOS Technology (1)

❑ About the Total Integrated Dose (TID)

In the past TID was requiring specially hardened process. The decreasing of the feature sizes of the present CMOS processes has resulted in a natural increase of the intrinsic hardness to TID and consequently does not really required a specific hardening (except if you really want a guaranteed TID hardness).

- ➢ Requirements for space applications may range from several 10 Krad to 100-300 Krad (we target 300 Krad).

Brief Status of the Radiation Hardness of CMOS Technology (2)

❑ About the Latch-Up (LU)

- Some processes are intrinsically LU free (such as the CMOS/SOS).

- Other processes (most of the commercial processes) require special process techniques to be LU free.
- But although some commercial process are sometimes LU free it may disappear from a lot to the next

➢ For space applications we target a LET of 100 MeV

Brief Status of the Radiation Hardness of CMOS Technology (3)

❑ About the Single Event Upset (SEU)

The decreasing of the feature sizes of the present CMOS processes has resulted in a significant increase of its intrinsic sensitivity to SEU

➢ Consequently we will concentrate the rest of the presentation on how we have designed microprocessors (in particular the LEON microprocessor) to decrease their sensitivity or even to make immune to SEU’s

Hardware Techniques for the SEU Hardening of Microprocessors

- use of intrinsic SEU insensitive process (CMOS/SOS)
- SEU detection (code protection such as parity to detect SEU’s as soon as possible to avoid error propagation)
- use of SEU hardened flip-flop (HDFF)
- error masking (Triple Modular Redundancy, TMR)

And a combination of some of the above techniques.
… the list is not exhaustive

Mapping of the SEU Design Techniques for the Implementation of the ESA Microprocessors

beg 90's	MA31750 (NMA31750)	2MIPS (16MHz)	**Use of intrinsic SEU insensitive technology: CMOS/SOS 1.25 micron**	• 300 KRad • LU insensitive • SEU insensitive
mid 90's	ERC32 chip-set (TSC691, TSC692, TSC693)	10MIPS (14MHz)	**Error detection with parity protection of registers**	• 50 Krad • LU insensitive • ~15 MeV LET for SEU
end 90's	ERC32 single chip (TSC695)	14MIPS (20MHz)	**Use of SEU Hardened F/F (the parity protection of registers was maintained)**	• 300 Krad • LU insensitive • 10^{-8} error/dev/day for SEU
beg 00's	LEON (TSC698)	100 MIPS	**TMR and use of ad hoc parity and EDAC**	• 300 Krad (TBC) • LU insensitive • SEU tolerant

SEU Fault Tolerant Design Techniques in LEON (1)

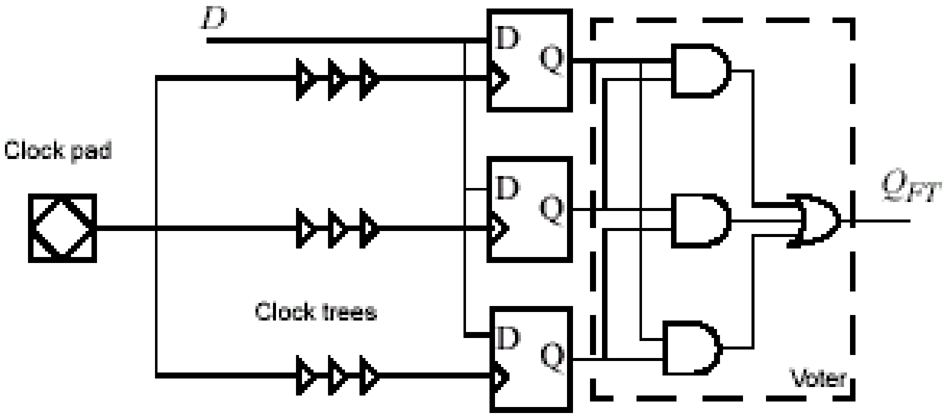
- ☐ TMR Registers
- ☐ On-chip EDAC
- ☐ Parity
- ☐ Pipeline restart
- ☐ Forced cache miss

SEU Fault Tolerant Design Techniques in LEON (2)

❖ Integer Unit	✓ TMR
❖ FPU	✓ TMR
❖ HW Multiplier and Divider	✓ TMR
❖ PCI controller	✓ TMR
❖ Cache controllers	✓ TMR
❖ Peripheral units	✓ TMR
❖ Debug Support Unit	✓ TMR
❖ Register File	✓ EDAC
❖ Cache memories	✓ Parity
❖ Trace Buffer	✓ NP
❖ JTAG	TBD

Use of TMR cell in LEON (1)

- ☐ The processor contains approximately 2,500 flip-flops used for temporary storage and state machines
- ☐ To protect against SEU errors each on-chip register is implemented using triple modular redundancy (TMR)



Use of TMR cell in LEON (2)

☐ The flip-flops are continuously clocked, and any SEU register error will automatically be removed within one clock cycle while the output of the voter will maintain the correct (glitch-free) value

☐ To further increase robustness, each of the three lanes of the TMR registers have separate clock-trees. An SEU hit in one clock-tree can therefore be tolerated even if the data of a complete lane of 2,500 registers is corrupted. On the following clock edge, all errors will be removed when new data is clocked in.

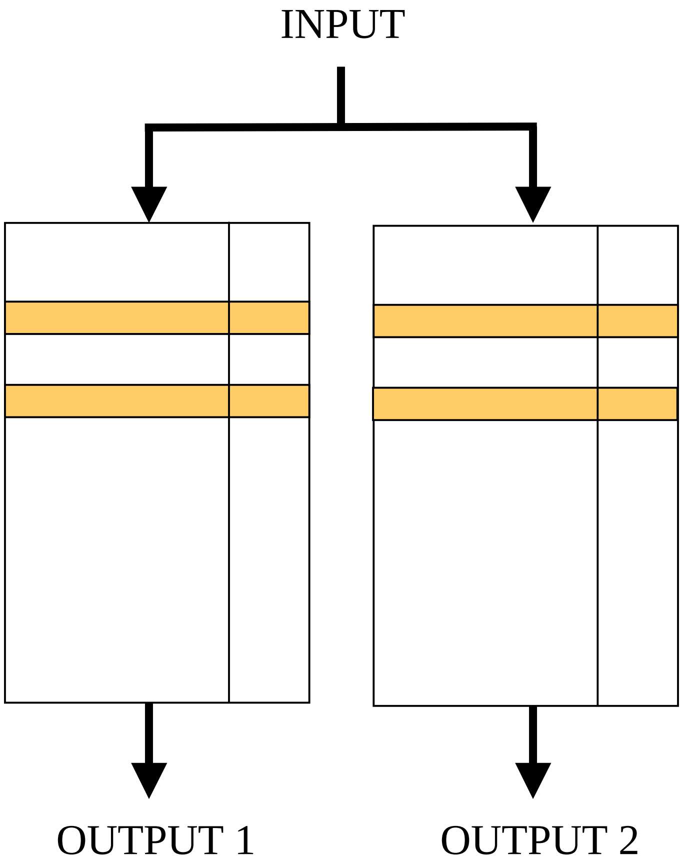
Use of TMR cell in LEON (3)

☐ Main Issues of Using TMR Cells

- ➢ Make sure that all the TMR cells are regularly refreshed to avoid double upset over long time period
- ➢ Feed the TMR cells with a skewed clock tree to avoid that a single hit on the clock tree may propagate to the three elements of the cells
  - problem: how much skew
  - penalty: it decreases the speed of operation
- ➢ Depending on which technique that is used for the TMR insertion you have to watch that the synthesis process do not defeat it

SEU Hardening of the LEON Register Files (1)

- The register file of LEON is 168 registers deep
- Since most standard-cell ram-libraries do not include three-port rams the register the file of LEON is then implemented as two parallel two-port rams with the write-ports connected together



SEU Hardening of the LEON Register Files (2)

- ☐ The LEON register file of LEON is protected by EDAC
- ☐ The protection bits are generated in the write stage of the pipeline and written together with the corresponding data
- ☐ The register file is read in the decode stage, but checking is done in the execute stage in parallel with instruction execution to avoid timing penalties in the decode stage
- ☐ If a correctable error is detected the pipeline is flushed and the erroneous operand data is corrected and written back to the register file (instead of the erroneous instruction result)
- ☐ The pipeline is then restarted at the point of the failing instruction (The time for the complete restart operation takes 4 clock cycles)
- ☐ If an uncorrectable error is detected a register error trap is generated.

SEU Hardening of the LEON Register Files (3)

- ☐ The register file has two read-ports and two error-detection units are implemented
- ☐ The register file has one write port and only one correction unit is needed
- ☐ If more than one correctable error occurs the instruction will be restarted once for each error, correcting and storing one register value each time
- ☐ In worst-case, a double-store instruction that use four individual registers can be restarted up to four times, correcting one register value at a time.

SEU Hardening of the LEON Caches

- For both instruction and data caches:

❖ Cache Controller	➢ TMR
❖ Cache Tag Memory	➢ Parity*
❖ Cache Data Memory	➢ Parity*

- The data cache uses write-through policy and a second copy of the data is thus always available
- A parity error is interpreted as a cache miss and the cache will be refilled from main memory according where the parity error has been detected
- No timing penalty occurs since parity checking is performed in parallel with tag checking.

* 2 parity bits per 32-bit word

LEON Synthesis Results on ATMEL ATC25

Module	Area nonFT (mm2)	Area with FT (mm2)	Overhead
Integer Unit (including Multiplier and Divider)	0.86	1.61	87 %
Cache Controllers	0.17	0.35	105 %
Peripherals Units	0.45	0.9	100 %
Register Files	0.19	0.24	26 %
Total	1.67	3.1	85 %

NOTE: it is not including the FPU, the PCI, the caches, and the DSU

LEON Development Status (1)

☐ The present LEON processor development ESA contract with ATMEL is divided in three phases:

- ➢ PHASE 1: Demonstrator
- ➢ PHASE 2: Prototype
- ➢ PHASE 3: Flight

LEON Development Status (2)

- The PHASE 1 Demonstrator was completed in Q2 2001
- A LEON demonstrator device made of the LEON core and the SUN (MEIKO) FPU was manufactured on 0.35 micron by ATMEL and was submitted successfully to heavy ions tests in Louvain facilities and has demonstrated the validity of the LEON fault-tolerant concept

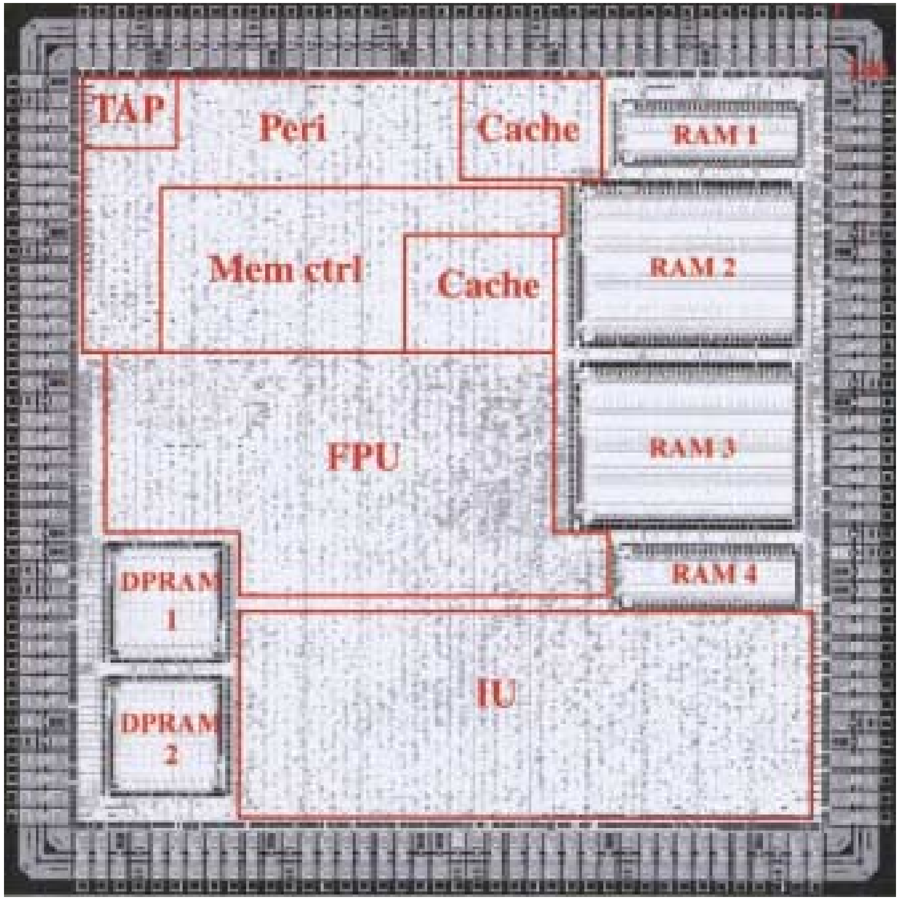
LEON Development Status (3)

- The PHASE 2 has just started in October 2002
- The first prototype devices are expected by the end July 2003
- The PHASE 3 (flight development) is foreseen to start beg. 2004
- The first flight devices are expected in Q3 2004

LEON Development Status (4)

- The time between the end of the Phase 1 and the start of the Phase 2 has been used to improve the design of LEON and to add some functionalities:
  - ☐ Cache snooping
  - ☐ SDRAM controller
  - ☐ DSU (Debug Support Unit, including a Trace Buffer)
  - ☐ Various design modifications and tunings to increase the speed of operation
- The last release of the complete VHDL model is the LEON-2 FT, version 1.04, dated 18 September 2002
- Final release for the implementation by ATMEL end November 2002

LEON Demonstrator 0.35 Micron Implementation



LEON Demonstrator device

LEON Demonstrator board for SEU testing

LEON Demonstrator SEU Test Results (1)

- ☐ The LEON Demonstrator was submitted to SEU testing @ 40 MHz and 3 V supply
- ☐ The test board was equipped with a test device and a reference device (master-checker mode) and using a dedicated test software
- ☐ The flux was 500 ions/cm2/sec
- ☐ The fluence was 1,000,000 per energy
- ☐ Energy range from 6 to 110 MeV

LEON Demonstrator SEU Test Results (2)

- ☐ The device SEU threshold was measured to be below 6 MeV
- ☐ The heavy-ion tests showed that for all the injected errors (> 100,000) the device correctly handled and recovered from all errors generated in sensitive internal elements without any software intervention.

Future LEON Improvements

☐ High Performance FPU

- pipe-lined FPU
- 100 MFLOPS
- design/validation has already been performed
- TMR to be implemented
- the implementation requires design changes to the core

☐ Memory Management Unit (@ the SPARC standard)

☐ Future implementation on 0.13 micron (target 200 MIPS)

Model Availability of LEON

- ❑ The VHDL model of LEON is available two versions:
  - ➢ A non Fault-Tolerant (nFT) model is publicly available under an open license
  - ➢ A Fault-Tolerant (FT) model available only to the countries that are member of the European Space Agency under an ESA license
- ❑ LEON will be available as a product (stand alone microprocessor) and as an IP core (use in SOC)
- ❑ ATMEL will have the exclusive license for the manufacturing of the LEON microprocessor on guaranteed radiation hardened technology

LEON Papers

- A Portable and Fault Tolerant Microprocessor Based on the SPARC V8 Architecture
- Hardware debug support in the LEON processor
- LEON DSU Monitor User’s Manual
- LEON2-FT Processor User’s Manual
  ADVANCE INFORMATION

LEON Contact persons

Mr A. L. R. Pouponnot	ESA/ESTEC TOS-ESD	apouponn@estec.esa.nl	(31) 71 565 3685	Technical Management.
Mr F. Mazzaglia	ESA/ESTEC IMT-CTE	Fabio.Mazzaglia@esa.int	(31) 71 565 5163	Contract Management, (incl. Licence)
Mr D. De Saint Roman	ATMEL Nantes	Dominique.de-saint-roman@nto.atmel.com	(33) 2 40 18 18 02	Marketing Management
Mrs V. Ho-Shui-Ling	ATMEL Nantes	Valerie.ho-shui-ling@nto.atmel.com	(33) 2 40 18 17 83	Project management
Mr J. Gaisler	Gaisler Research	Jiri@gaisler.com	(46) 31 802 405	Design LEON core
Mr R. Weigand	ESA/ESTEC TOS-ESM	Roland.Weigand@esa.int	(31) 71 565 3298	Design PCI

URL Addresses

ESA:

http://www.esa.int
http://www.estec.esa.int/microelectronics/components/comppage.html
http://www.estec.esa.int/microelectronics/core/corepage.html

ERC32 and LEON:

http://www.atmel.com
http://www.gaisler.com

MA31750
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